P1P40167

1.8V, 4-PLL Low Power Clock Generator with Spread Spectrum

ON Semiconductor®

http://onsemi.com

Functional Description

The P1P40167 is a high precision frequency synthesizer designed to operate with a 27 MHz fundamental mode crystal. Device has 4 PLL's with four LVCMOS outputs and a reference clock. The frequencies generated are 22.5792 MHz, 24.576 MHz, 48 MHz and 37 MHz as well as a 27 MHz copy of the reference clock. Device offers flexible spread spectrum options configurable through I^2C bus. All output clocks are generated with high precision, zero PPM frequency conversion, thus making it suitable for high−end multimedia and consumer applications. I^2C is included to support various system configuration options.

Features

- Low Power Architecture to Support Portable Applications
- Integrated Loop Filter
- Input: 27 MHz Crystal or External Input
- Outputs:
  - 27 MHz Reference Output
  - Fixed Output Frequencies of 48 MHz and 22.5792 MHz
  - Configurable Spread Spectrum for 37 MHz Output
  - Selectable Audio Clock Frequency of Either 22.5792 MHz or 24.576 MHz
- LVCMOS Input and Outputs
- Supply Voltage: 1.8 V
- 16−pin QFN Package
- Operating Temperature Range: −10°C to +80°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Portable Gaming
- Audio/Video Multimedia

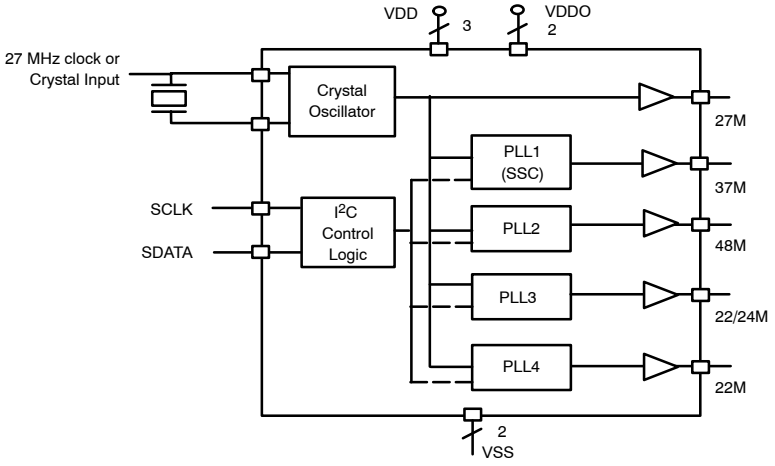


Figure 1. Block Diagram

MARKING DIAGRAM

QFN16
CASE 485G

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

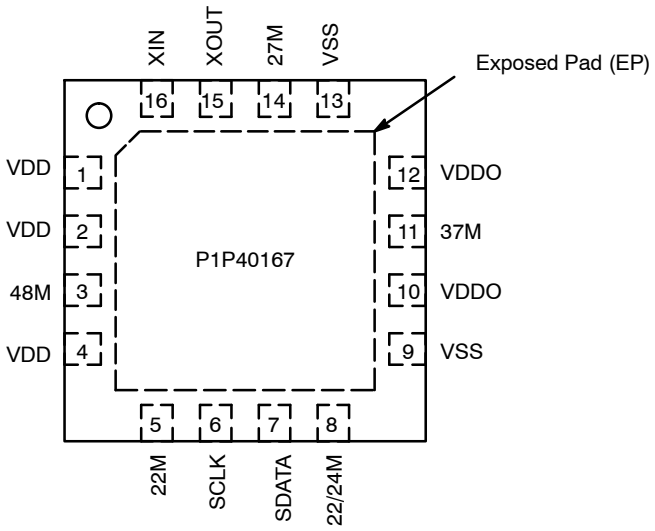


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	VDD	Power	1.8 V power supply for Core
2	VDD	Power	1.8 V power supply for Core
3	48M	Output	48 MHz clock output. Has internal pull down resistor.
4	VDD	Power	1.8 V power supply for Core
5	22M	Output	22.5792 MHz clock output. Has internal pull down resistor.
6	SCLK	Input	I^2C bus Clock input, internal pull−up resistor
7	SDATA	Input / Output	I^2C bus Data pin, Internal pull−up resistor
8	22/24M	Output	24.576 MHz or 22.5792 MHz clock output. Has internal pull down resistor.
9	VSS	Power	0 V device ground
10	VDDO	Power	1.8 V power supply for Output Clocks
11	37M	Output	37 MHz clock output. Has internal pull down resistor.
12	VDDO	Power	1.8 V power supply for Output Clocks
13	VSS	Power	0 V device ground
14	27M	Output	Buffered 27 MHz reference clock output. Has internal pull down resistor.
15	XOUT	Output	Crystal connection. If using an external reference, this pin must be left unconnected.
16	XIN	Input	Crystal connection. Connect to 27 MHz crystal or External clock input
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The pad is electrically connected to the die, and can be electrically and thermally connected to device ground on the PC board.

EXTERNAL COMPONENTS

Decoupling Capacitor

As with any high−performance mixed−signal IC, the P1P40167 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.1 μF must be connected between each VDD and the PCB ground plane.

I²C External Resistor Connection

The SCLK and SDATA pins can be connected to any voltage between 1.8 V and 2.0 V.

Crystal Load Capacitors

No external crystal load capacitors are required. To save discrete component cost, the P1P40167 integrates on−chip capacitance to support a crystal with C_L = 10.5 pF. It is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device.

Table 2. ABSOLUTE MAXIMUM RATING

Symbol	Parameter		Rating	Unit
VDD / VDDO	Supply Voltage		−0.5 to 3.6	V
V_{IN}	All Inputs		−0.5 to (VDD + 0.5)	V
V_{OUT}	All Outputs		−0.5 to (VDDO + 0.5)	V
T_A	Storage Temperature		−65 to +150	°C
T_J	Junction Temperature		125	°C
T_S	Soldering Temperature		260	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22−A114−B)	Human Body Model	2000	V
		Machine Model	200	
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm	42	°C/W
		500 lpfm	35	
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 1)		4.0	°C/W
MSL	Moisture Sensitivity Level		1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min	Typ	Max	Unit
VDDO	Operating Supply Voltage (Output Clocks)	1.7	1.8	2.0	V
VDD	Operating Supply Voltage (Core)	1.7	1.8	2.0	V
T_A	Ambient Operating Temperature	−10		+80	°C

Table 4. DC ELECTRICAL CHARACTERISTICS
Unless stated otherwise, VDD/VDDO = 1.8 V − 0.1 V/+0.2 V, T_A = −10°C to +80°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD / VDDO	Supply Voltage		1.7		2.0	V
I_{DD}	Power Supply Current	No Load, VDD, VDDO = 1.8 V, All output clocks running and spread ON		10	12	mA
V_{IH}	Input High Voltage		0.7 x VDD			V
V_{IL}	Input Low Voltage				0.3 x VDD	V
V_{OH}	Output High Voltage	I_{OH} = −2 mA	0.8 x VDDO			V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.2 x VDDO	V
C_{IN}	Input Capacitance	Except XIN, XOUT pins		5		pF
C_{LOAD}	Xtal Load Capacitance	XIN, XOUT		10.5		pF
R_{PU}	Internal Pull−up Resistor	SCLK, SDATA Pins	100	500		kΩ
R_{PD}	Internal Pull−down Resistor	22M, 22/24M, 27M, 37M, 48M	75	250		kΩ

Table 5. AC ELECTRICAL CHARACTERISTICS (Note 2)
(Unless stated otherwise, VDD/VDDO = 1.8 V −0.1 V/+0.2 V, C_L = 5 pF, T_A = −10°C to +80°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fin	Input Frequency			27		MHz
T_F / T_R	Output Rise / Fall Time	Measured between 20% and 80%	1.1	1.8	3.3	ns
R_O	Output Impedance	VO = VDDO /2		104		Ω
T_{DC27}	Output Clock Duty Cycle	27 MHz output @VDDO/2	45	50	55	%
T_{DC}		37 MHz, 48 MHz, 22/24 MHz and 22.5792 MHz clocks @ VDDO/2	45	50	55	%
	Freq Synthesis Error	All Outputs		0		ppm
T_{PJ}	Absolute Clock Period Jitter			±225	±400	ps
T_{CCJ}	Cycle to Cycle Jitter			225	375	ps
T_{LTJ1}	Long Term Jitter	27 MHz, n = 1000			750	ps
T_{LTJ2}		48 MHz, n = 1000			750	ps
T_{LTJ3}		22 MHz and 22/24MHz, n=1000			1500	ps
T_{LTJ4}		37 MHz with SSOFF n = 20, sample count = 3k		550	750	ps
T_{WAIT}	22/24M Clock Switching Time	Finish from prior cycle to start of new cycle			15	μs
T_{PU}	Power−up Time	From minimum VDD to outputs stable		1.5	4.0	ms
t_{OEEN}	Output Enable Time	Measured from rising edge of last I^2C clock			20	μs
		22/24M, Measured from rising edge of last I^2C clock			150	μs
		37M, Measured from rising edge of last I^2C clock			1.5	ms
t_{OEZ}	Output Disable Time	Measured from rising edge of last I^2C clock			20	μs
	Crystal Power			200		μW

2. Guaranteed by design, not tested in production.

SERIAL DATA INTERFACE

Data Protocol

The Clock Driver serial protocol accepts byte write, byte read, block write, and block read operations from the Controller. For Block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code as described in the following table.

Bit	Description
7	0= Block read or Block write operation, 1= Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For Block read or Block write operations, these bits should be ‘0000000’.

The Block write and Block read protocol is outlined in the table below, followed by the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command code – 8 bit ‘00000000’ stands for block operation	11:18	Command code – 8 bit ‘00000000’ stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge from master
…...	……	39:46	Data byte from slave – 8 bits
…...	Data byte (N–1) – 8 bits	47	Acknowledge from master
…...	Acknowledge from slave	48:55	Data byte from slave – 8 bits
…...	Data byte N – 8 bits	56	Acknowledge from master
…...	Acknowledge from slave	…..	Data byte N from slave – 8 bits
…...	Stop	…..	Not Acknowledge from master
		….	Stop

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave addresses – 7 bits	2:8	Slave addresses – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command code – 8 bit '10000000' stands for byte operation, bits[1:0] command code represents the offset of the byte to be accessed	11:18	Command code – 8 bit '10000000' stands for byte operation bits[1:0] command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38 39	Not Acknowledge from master stop

Byte 0: Vendor ID, Revision Code

Bit	@Pup	Name	Description
7	0	Revision Code (MSB)	Revision Code
6	0	Revision Code	Revision Code
5	0	Revision Code	Revision Code
4	1	Revision Code (LSB)	Revision Code
3	1	Vendor ID (MSB)	Vendor ID
2	1	Vendor ID	Vendor ID
1	0	Vendor ID	Vendor ID
0	0	Vendor ID (LSB)	Vendor ID

Byte 1 Controller Register

Bit	@Pup	Name	Description
7	1	27M	27M Output Enable 0 = Disable (Output pulled LOW), 1= Enable
6	1	37M	37M Output Enable 0 = Disable (Output pulled LOW), corresponding PLL shut off. 1= Enable
5	1	48M	48M Output Enable 0 = Disable (Output pulled LOW), 1= Enable
4	1	22/24M	22/24M Clock Output Enable 0 = Disable (Output pulled LOW), 1= Enable
3	0	22M	22M Output Enable 0 = Disable (Output pulled LOW), 1= Enable
2	1	Reserved	Reserved
1	1	Reserved	Reserved
0	1	22/24M SEL	22/24M Clock Select 1= 24.576 MHz, 0= 22.5792MHz

Byte 2 Controller Register

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	SS Table	Bit 2:0 = 000: No Spread Bit 2:0 = 001: – 0.5% Spread Bit 2:0 = 010: – 1.0% Spread Bit 2:0 = 011: No Spread Bit 2:0 = 100: –2.0%Spread Bit 2:0 = 101: No Spread Bit 2:0 = 110: –3.0%Spread Bit 2:0 = 111: No Spread
1	1	SS Table	
0	0	SS Table	

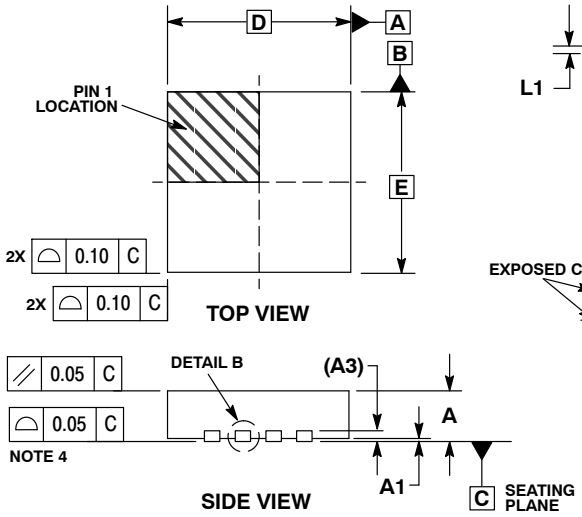
ORDERING INFORMATION

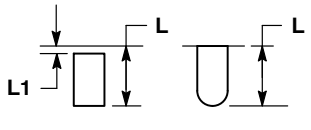
Part Number	Package Type	Shipping†
P1P40167MNTWG	QFN16 (Pb–Free)	3000 / Tape & Reel

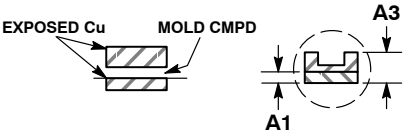
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F

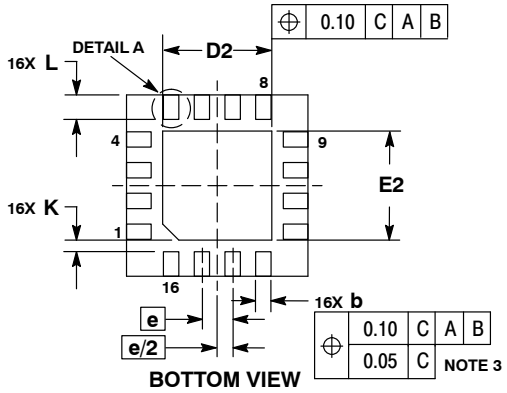




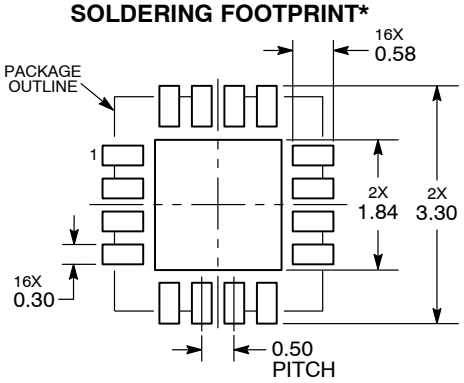


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
K		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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