

# 3.3V Dual LVTTL/LVCMOS-to-Differential MC100ES60T22 **LVPECL** Translator

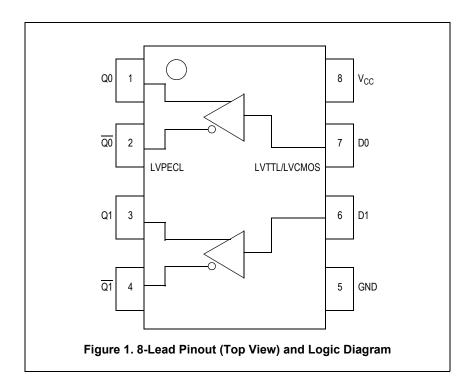
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**DATA SHEET** 

The MC100ES60T22 is a low skew dual LVTTL/LVCMOS to differential LVPECL translator. The low voltage PECL levels, small package, and dual gate design are ideal for clock translation applications.

#### **Features**

- 280 ps typical propagation delay
- 100 ps max output-to-output skew
- LVPECL operating range:  $V_{CC}$  = 3.135 V to 3.8 V
- 8-lead SOIC and 8-lead TSSOP packages
- Ambient temperature range -40°C to +85°C
- 8-lead SOIC Pb-free package available





D SUFFIX **8-LEAD SOIC PACKAGE CASE 751-07** 

**EF SUFFIX 8-LEAD SOIC PACKAGE Pb-FREE PACKAGE CASE 751-07** 



**DT SUFFIX 8-LEAD TSSOP PACKAGE CASE 1640-01** 

**EJ SUFFIX 8-LEAD SOIC PACKAGE Pb-FREE PACKAGE CASE 1640-01** 

ORDERING INFORMATION					
Device	Package				
MC100ES60T22D	SOIC-8				
MC100ES60T22DR2	SOIC-8				
MC100ES60T22EF	SOIC-8 (Pb-Free)				
MC100ES60T22EFR2	SOIC-8 (Pb-Free)				
MC100ES60T22DT	TSSOP-8				
MC100ES60T22DTR2	TSSOP-8				
MC100ES60T22EJ	TSSOP-8 (Pb-Free)				
MC100ES60T22EJR2	TSSOP-8 (Pb-Free)				

PIN DESCRIPTION						
Pin Function						
D0, D1	LVTTL/LVCMOS Inputs					
Qn, Qn	LVPECL Differential Outputs					
V <sub>CC</sub>	Positive Supply					
GND	Negative Supply					

**Table 1. General Specifications** 

Charac	Value		
Internal Input Pulldown Resistor	75 kΩ		
Internal Input Pullup Resistor	ut Pullup Resistor		
ESD Protection	Human Body Model Machine Model	> 2000 V > 200 V	
$\theta_{JA}$ Thermal Resistance (Junction-to-Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC 0 LFPM, 8 TSSOP 500 LFPM, 8 TSSOP	190°C/W 130°C/W 185°C/W 140°C/W	

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Conditions	Rating	Units
V <sub>SUPPLY</sub>	Power Supply Voltage	Difference between V <sub>CC</sub> & V <sub>EE</sub>	3.9	V
V <sub>IN</sub>	Input Voltage	$V_{CC} - V_{EE} \le 3.6 \text{ V}$	V <sub>CC</sub> + 0.3 V <sub>EE</sub> - 0.3	V V
l <sub>out</sub>	Output Current	Continuous Surge	50 100	mA mA
$T_A$	Operating Temperature Range		-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C

Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these
conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated
conditions is not implied.

Table 3. DC Characteristics ( $V_{CC}$  = 3.135 V to 3.8 V;  $V_{EE}$  = 0 V)

			-40°C		0°C to 85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Unit
V <sub>OH</sub> <sup>(1)</sup>	Output HIGH Voltage	V <sub>CC</sub> – 1150	V <sub>CC</sub> – 1020	V <sub>CC</sub> – 800	V <sub>CC</sub> – 1200	V <sub>CC</sub> – 970	V <sub>CC</sub> – 750	mV
V <sub>OL</sub> <sup>(1)</sup>	Output LOW Voltage	V <sub>CC</sub> – 1950	V <sub>CC</sub> – 1620	V <sub>CC</sub> – 1250	V <sub>CC</sub> – 2000	V <sub>CC</sub> – 1680	V <sub>CC</sub> – 1300	mV

<sup>1.</sup> Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC}$  – 2 volts.

Table 4. LVTTL / LVCMOS Input DC Characteristics ( $V_{CC}$  = 3.135 V to 3.8 V)

				-40°C		0°C to 85°C			
Symbol	Characteristic	Condition	Min	Тур	Max	Min	Тур	Max	Unit
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = V <sub>CC</sub>			±150			±150	μА
V <sub>IK</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA			-1.2			-1.2	V
V <sub>IH</sub>	Input HIGH Voltage		2.0		V <sub>CC</sub> +0.3	2.0		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage				0.8			0.8	V

Table 5. AC Characteristics ( $V_{CC}$  = 3.134 V to 3.8 V;  $V_{EE}$  = 0 V)

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f <sub>max</sub>	Maximum Toggle Frequency			1			1			1	GHz
t <sub>PLH,</sub> t <sub>PHL</sub>	Propagation Delay	100	260	400	100	280	400	100	280	450	ps
t <sub>SKEW</sub>	Skew part-to-part			300			300			350	ps
t <sub>JITTER</sub>	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V <sub>outPP</sub>	Output Peak-to-Peak Voltage	350	750		350	750		350	750		mV
t <sub>r</sub> / t <sub>f</sub>	Output Rise/Fall Times (20% – 80%)	50		400	50		400	50		400	ps

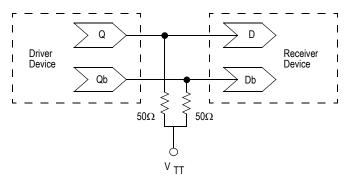
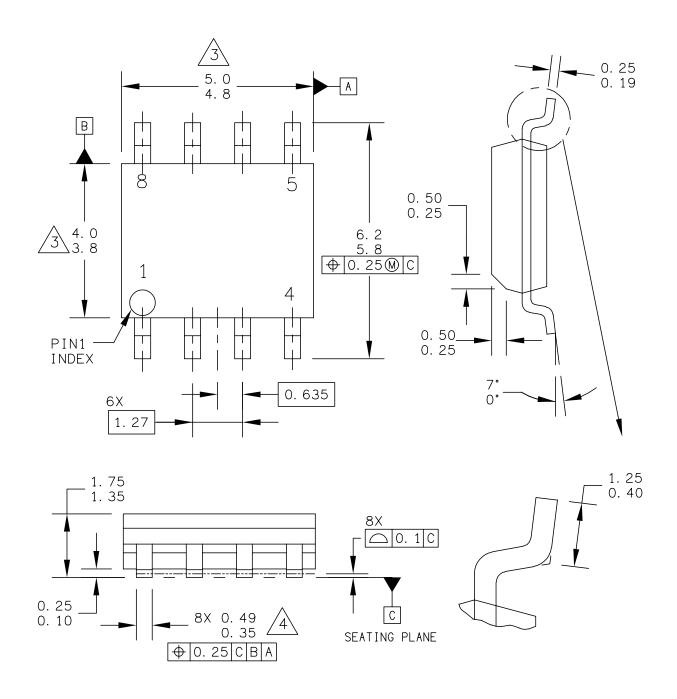


Figure 2. Typical Termination for Output Driver and Device Evaluation

## **PACKAGE DIMENSIONS**



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TITLE:		DOCUMENT NO	): 98ASB42564B	REV: U
8LD SOIC NARROW	BODY	CASE NUMBER	2: 751–07	07 APR 2005
		STANDARD: JE	DEC MS-012AA	PAGE 1 OF 2

CASE 751-07 ISSUE U 8-LEAD SOIC PACKAGE

## PACKAGE DIMENSIONS

#### NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

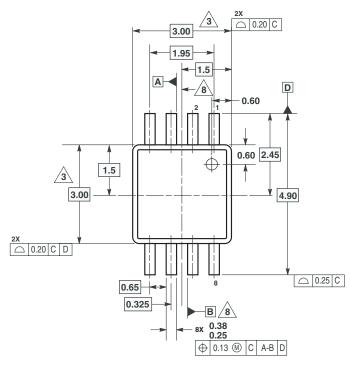
DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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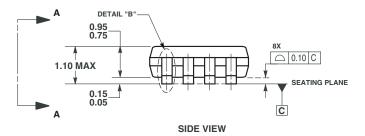
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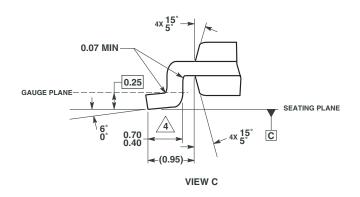
**CASE 751-07 ISSUE U 8-LEAD SOIC PACKAGE** 

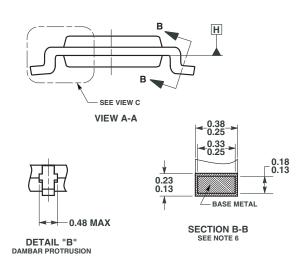
## **PACKAGE DIMENSIONS**



**TOP VIEW** 







#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. DIMENSIONS ARE IN MILLIMETERS.
- 3 THIS DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT DATUM H, MOLD FLASH OR PROTRUSIONS, SHALL NOT EXCEED 0.15mm PER SIDE.
- DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
  ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS
  OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
  DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD
  FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD
  TO BE 0.14mm SEE DETAIL "B" AND SECTION B-B.
- SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25mm FROM THE LEAD TIP.
- 7. THIS PART IS COMPLIANT WITH JEDEC REGISTRATION MO-187 AA.

  8. DATUMS A AND B TO BE DETERMINED DATUM PLANE H.

CASE 1640-01 ISSUE O 8-LEAD TSSOP PACKAGE



6024 Silver Creek Valley Road San Jose, California 95138 **Sales** 800-345-7015 (inside USA) +408-284-8200 (outside USA) Fax: 408-284-2775 www.IDT.com/go/contactIDT Technical Support netcom@idt.com +480-763-2056

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