PIC18F6585/6680/8585/8680

PIC18F6585/6680/8585/8680 Rev. A1 Silicon Errata

The PIC18F6585/6680/8585/8680 Rev. A1 parts you have received conform functionally to the Device Data Sheet (DS30491**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6585/6680/8585/8680 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F6585/6680/8585/8680 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6585	0000 1010 011	0 0001
PIC18F6680	0000 1010 001	0 0001
PIC18F8585	0000 1010 010	0 0001
PIC18F8680	0000 1010 000	0 0001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

All the issues listed here will be addressed in future revisions of the PIC18F6585/6680/8585/8680 silicon.

1. Module: EUSART

If the transmitter is left enabled while the module is performing an auto-baud operation, an arbitrary data byte may get transmitted.

Work around

Clear TXEN (TXSTA<5>) before any auto-baud operation and set it after auto-baud is complete.

Enable TXEN only when a data byte is to be transmitted. Care must be taken to ensure that the TX pin is pulled high, either through an external resistor, or by making the TX pin an output and writing '1' to it to not disturb the transmit line.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: EUSART

This module may perform incorrect auto-baud calculation if the ABDEN (BAUDCON<0>) bit was set while the receive pin was at a low level.

Work around

Wait for the RX pin to go high and then set the ABDEN bit.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: EUSART

In Asynchronous Receiver mode, the EUSART does not load the SPBRGH value after completion of auto-baud.

Work around

Do not enable the BRG16 (BAUDCON<3>) bit.

If the BRG16 is in use, ensure that the auto-baud SPBRG value does not exceed the 8-bit value.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: EUSART

The CREN (RCSTA<4>) bit is cleared after every auto-baud operation.

Work around

Upon completion of auto-baud, manually set the CREN bit.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: CCP2

CCP2CON<3:0> value of '1110' or '1111' produces incorrect PWM output.

Work around

Use CCP2CON<3:0> value of '110x' for PWM mode.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Enhanced Controller Area Network (ECAN™ Technology)

In Mode 2, the $\overline{\text{FIFOEMPTY}}$ bit (COMSTAT<7>) is not automatically cleared upon a FIFO empty condition.

Work around

Clear $\overline{\text{FIFOEMPTY}}$ bit twice after reading any message from FIFO. $\overline{\text{FIFOEMPTY}}$ will remain set if FIFO is still not empty.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: Enhanced Controller Area Network (ECAN™ Technology)

Bits 7 and 6 in the COMSTAT register are swapped for write operation. As a result, performing an individual set/clear bit operation on bit 6 in the COMSTAT register actually sets/clears bit 7 and vice versa. Note that the read operation will read the correct bit.

Work around

If individual bit clear operation is required, first make sure that the desired bit is not already cleared. If the bit is set, use the swapped bit position. For example, use '`BCF COMSTAT, 6`' to clear bit 7. If the bit is already cleared, do not clear it again.

If possible, operate on the entire register using '`MOVWF`, `MOVFF`, `CLRF`', etc. instructions.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: ADC

A/D conversion does not start if the device is put to Sleep during the auto-acquisition period. As a result, the device will need another wake-up event source to wake-up from Sleep.

Work around

Do not use the auto-acquisition feature when A/D conversion during Sleep is required.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: Core (Instruction Set)

The Decimal Adjust W register instruction, `DAW`, may improperly clear the Carry (C) bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the `DAW` instruction. If the Carry bit is set, increment the next higher byte to be added using an instruction such as `INCFSZ` (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the `DAW` instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
```

This is repeated for each `DAW` instruction.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: Enhanced Controller Area Network (ECAN™ Technology)

The behavior of the Phase Segment 2 Select bit (SEG2PHTS) in the BRGCON2 register is inverted. As a result, when Phase Segment 2 is less than Phase Segment 1, or IPT, the actual bit rate will not be correct.

Work around

1. Use SEG2PHTS = `0` for freely programmable and '`1`' for maximum of Phase Segment 1 or Information Processing Time (IPT), whichever is greater.
2. Select Phase Segment 2 such that it is greater or equal to Phase Segment 1.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: Enhanced Controller Area Network (ECAN™ Technology)

Bit ERRIF in the PIR3 register is incorrectly set when a message is received in Mode 2. This may incorrectly indicate an error condition on the bus. When ERRIF is incorrectly set, a sequence of steps must be followed to clear the incorrect ERRIF flag.

Work around

To determine the correct error state, do the following checks:

1. If any of the COMSTAT<5:0> bits are non-zero, an error condition has occurred.
2. Otherwise, an error did not occur.

To remove the incorrect error state, do the following:

1. Clear $\overline{\text{FIFOEMPTY}}$ bit.
2. Clear ERRIF bit.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: EUSART

Bit SENDB in the TXSTA register is not automatically cleared by hardware upon completion of transmission of a Sync Break.

Work around

Check the TRMT bit in TXSTA. If TRMT bit is set, Break transmission is said to be complete.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: External Memory Interface

When performing writes on the external memory interface, a short glitch is present on the $\overline{\text{LB}}$ and $\overline{\text{UB}}$ lines. The length of the glitch is proportional to FOSC and may vary with process, voltage and temperature. The glitch occurs well before the $\overline{\text{WRH}}$ signal is asserted and no adverse affect on the operation of the external memory interface has been observed.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: Core

Certain combinations of code sequence, code placement, VDD, FOSC and temperature may cause a corrupted read of fetched instructions or data. A corrupted instruction fetch will cause the part to execute an incorrect instruction with unpredictable results.

Microchip cannot predict which combinations of these conditions will cause this failure.

If this failure mechanism exists in your system, it should become evident during statistically significant preproduction testing, using your particular code sequence and placement, across multiple date codes. Preproduction testing should exercise all the functions of your application across system variables. Any changes to code should be tested in the same manner prior to being implemented.

Work around

- Try changing the placement of code within program memory. Examples of code placement changes include:
  - Insert a data word of value FFFFh immediately following any table read instruction
  - Insert a data word of value FFFFh as the first instruction in the destination of a `CALL` or `GOTO`
  - Insert a data word of FFFFh at the interrupt vector address(es) (0008h and/or 0018h)
  - Insert a data word of value FFFFh immediately following any `RETURN`, `RETLW`, or `RETFIE` instruction

In each of these instances, the literal data behaves as a `NOP` instruction when it is executed. Using the actual `NOP` instruction instead of a literal FFFFh may not have the same results.

After making any of the changes described above, it is necessary that you do statistically significant preproduction testing, using your new code sequence and placement, across multiple date codes. Preproduction testing should exercise all the functions of your application across system variables.

- Contact your nearest Microchip sales office for additional help.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: Enhanced Controller Area Network (ECAN™ Technology)

Under specific conditions, the first five bits of a transmitted identifier may not match the value in the Transmit Buffer ID register, TXBnSIDH. The following conditions must exist for the corruption to occur:

- A transmit message must be pending.
- The ECAN module must detect a Start-of-Frame (SOF) in the third bit of interframe space.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: Enhanced Controller Area Network (ECAN™ Technology)

Under specific conditions, the TXBnSIDH register of the pending message for transmission may be corrupted. The following conditions must exist for this event to occur:

- A transmit message must be pending.
- All of the receive buffers must be full with a received message in the Message Assembly Buffer (MAB).
- A receiver buffer must be made available (RXBnCON<RXFUL> set to '0') at one of the following times:
  - When a Start-of-Frame (SOF) is recognized on the CAN bus.
  - On the instruction cycle prior to the SOF.

  The timing of this event is crucial.

Work around

Ensure that a receive buffer overflow condition does not occur and/or ensure that a transmit request is not pending if a receive buffer overflow condition does exist.

The pseudo code segment in Example 2 is an example of how to disable a pending transmission. This code is for illustration purposes only.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 2:

```
If (RXBnOVFL == 1)                // Has an overflow occurred?
        {   If (TXREQ == 1)       // Is a transmission pending?
            {   TXREQ = 0;        // Clear transmit request
                If (TXABT == 1)   // Store transmission aborted status value
                    MyFlag = 1;
            }
        }
        Temp_RXREG = RXBx;        // Read receive buffer
        If (MyFlag)               // Was previous transmission aborted?
        {   TXREQ = 1;            // Set transmit request
            MyFlag = 0;           // Reset stored transmission aborted status
        }
```

REVISION HISTORY

Rev A Document (7/2003)
First revision of this document, silicon issues 1 through 4 (EUSART), 5 (CCP2), 6 and 7 (ECAN™ Technology), 8 (ADC) and 9 (Core) and data sheet clarification issue 1 (Oscillator) and 2 (MCLRE Bit).

Rev B Document (9/2003)
Added silicon issue 10 (ECAN™ Technology).

Rev C Document (12/2003)
Added silicon issue 11 (ECAN™ Technology), 12 (EUSART) and 13 (External Memory Interface).

Rev D Document (12/2006)
Added silicon issue 14 (Core).

Rev E Document (8/2007)
Removed data sheet clarifications and retitled document as silicon errata. Added silicon issues 15 and 16 (ECAN™ Technology). Corrected silicon issue titles for ECAN Technology.

NOTES:

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