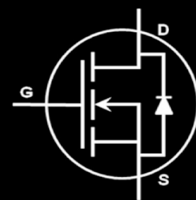
EPC2025 – Enhancement Mode Power Transistor

V_{DSS} , 300 V
$R_{DS(on)}$, 120 mΩ
I_D , 6.3 A

NEW PRODUCT

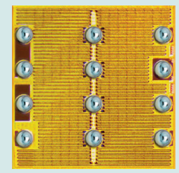


EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	300	V
I_D	Continuous (T_A = 25˚C, $R_{\Theta JA}$ = 13˚C/W)	6.3	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	20	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	



EPC2025 eGaN® FETs are supplied only in passivated die form with solder bumps
Die Size: 1.95 mm x 1.95 mm

Applications
- Ultra High Frequency DC-DC conversion
- Medical
- Solar
- LED Lighting

Benefits
- Ultra High Efficiency
- Ultra Low Switching and Conduction Losses
- Zero Q_{RR}
- Ultra small footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2025.aspx

Static Characteristics (T_J = 25˚C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 120 µA	300			V
I_{DSS}	Drain Source Leakage	V_{DS} = 240 V, V_{GS} = 0 V		20	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.1	2	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		20	100	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 3 A		90	120	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		2.5		V

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	**UNIT**
$R_{\Theta JC}$	Thermal Resistance, Junction to Case	1.6	˚C/W
$R_{\Theta JB}$	Thermal Resistance, Junction to Board	9.5	˚C/W
$R_{\Theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	64	˚C/W

Note 1: $R_{\Theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J = 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 240 V, V_{GS} = 0 V		200	240	pF
C_{RSS}	Reverse Transfer Capacitance			0.1		
C_{OSS}	Output Capacitance			46	70	
$C_{OSS(ER)}$	Effective Output Capacitance Energy Related (Note 2)	V_{DS} = 0 to 240 V, V_{GS} = 0 V		64		
$C_{OSS(TR)}$	Effective Output Capacitance Energy Related (Note 3)			93		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 240 V, V_{GS} = 5 V, I_D = 3 A		1.8	2.3	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 240 V, I_D = 3 A		0.72		
Q_{GD}	Gate-to-Drain Charge			0.32	0.54	
$Q_{G(TH)}$	Gate Charge at Threshold			0.54		
Q_{OSS}	Output Charge	V_{DS} = 240 V, V_{GS} = 0 V		22	33	
Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 80% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

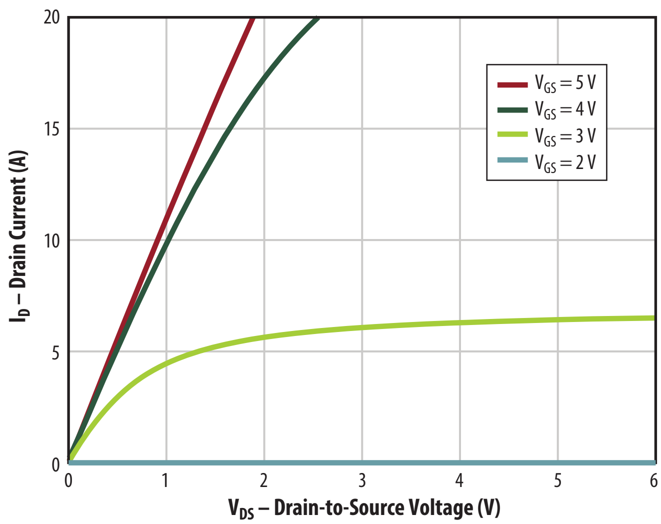


Figure 2: Transfer Characteristics

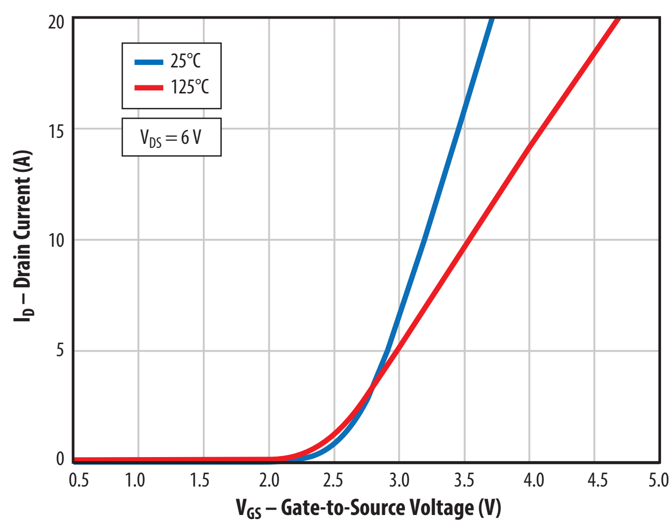


Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Drain Currents

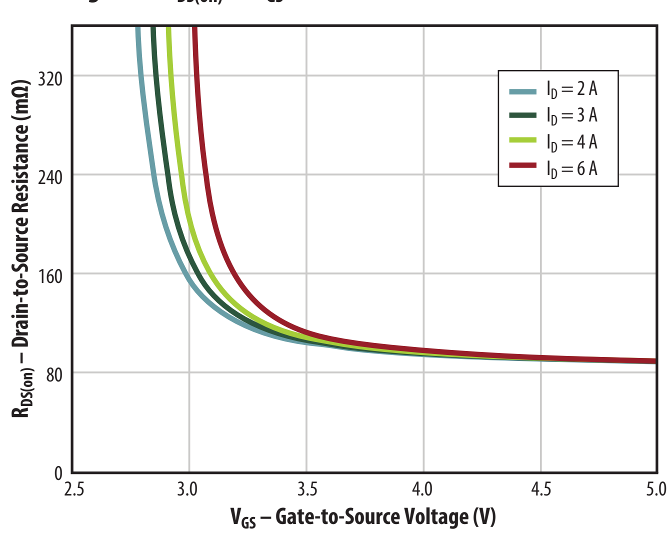


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperatures

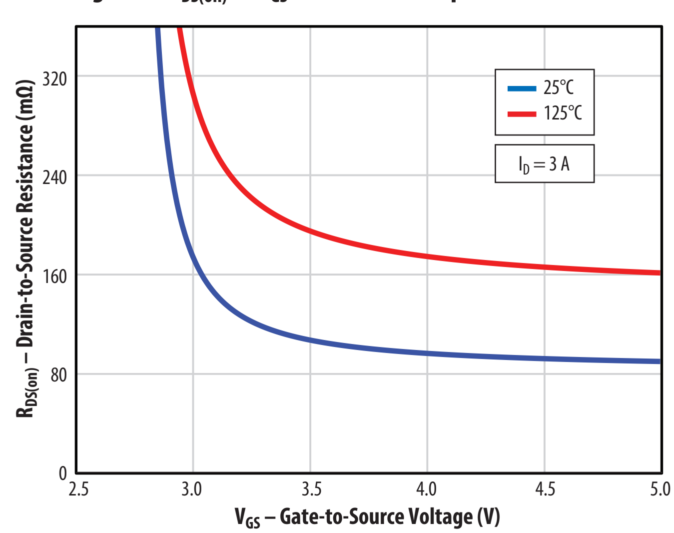


Figure 5a: Capacitance (Linear Scale)

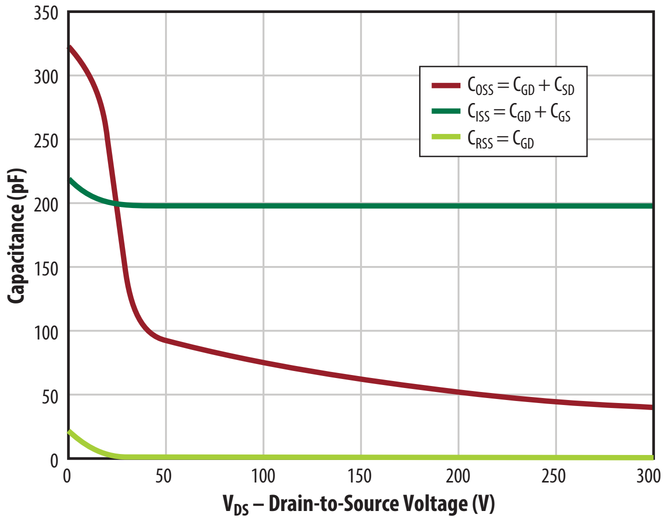


Figure 5b: Capacitance (Log Scale)

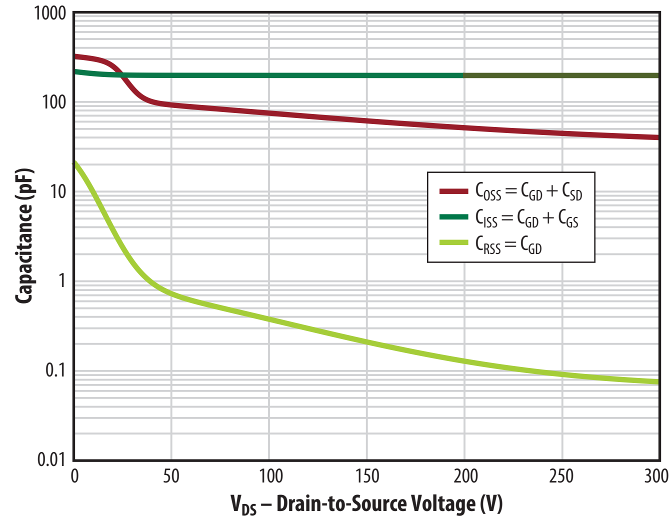


Figure 6: Gate Charge

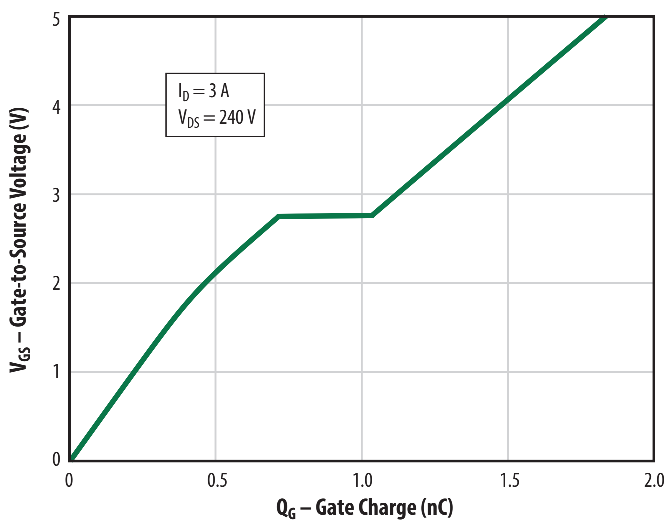


Figure 7: Reverse Drain-Source Characteristics

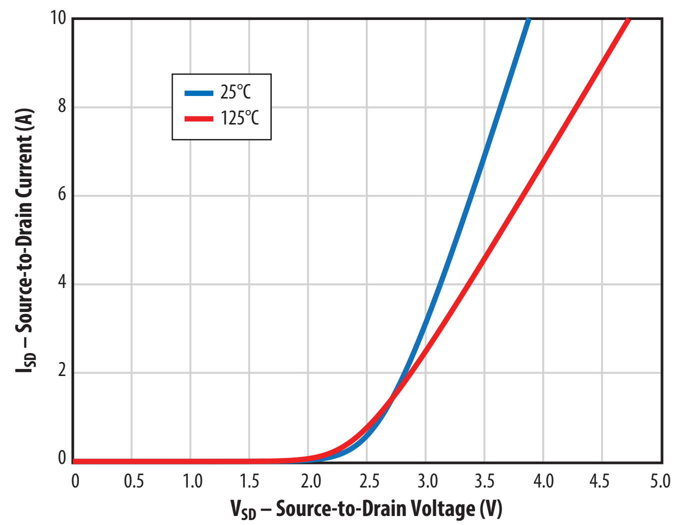


Figure 8: Normalized On-State Resistance vs Temperature

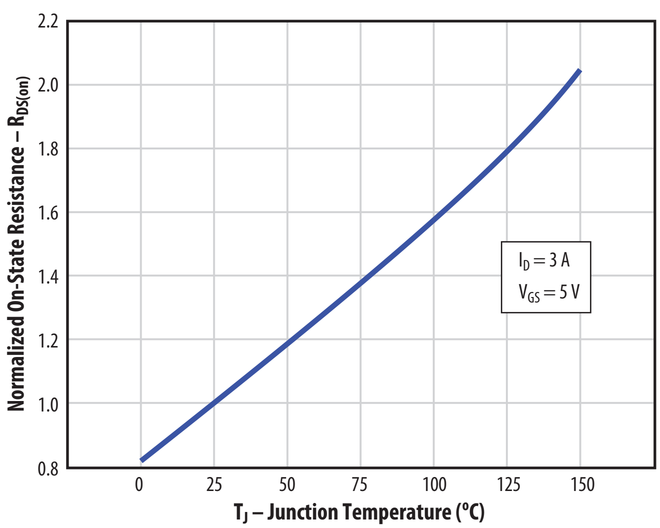
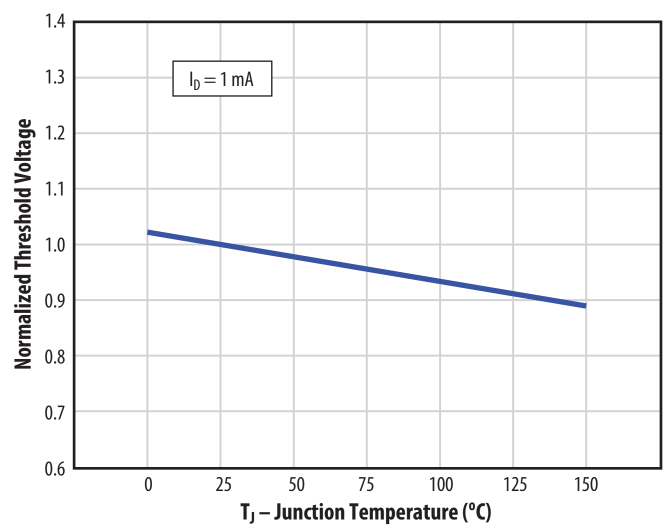


Figure 9: Normalized Threshold Voltage vs Temperature



All measurements were done with substrate shortened to source.

Figure 10: Gate Leakage Current

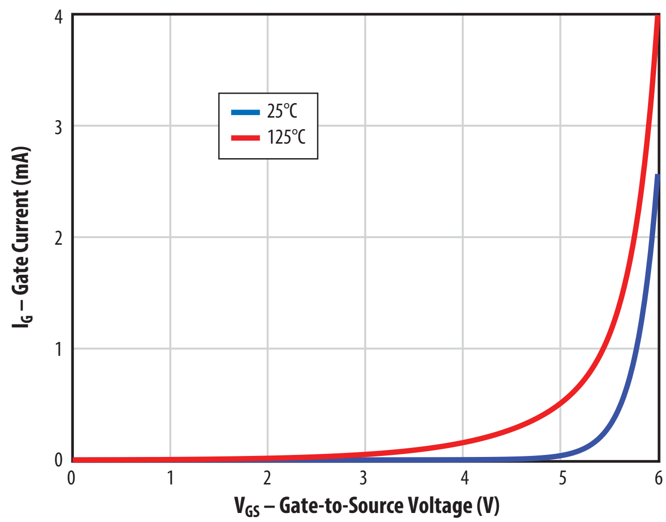
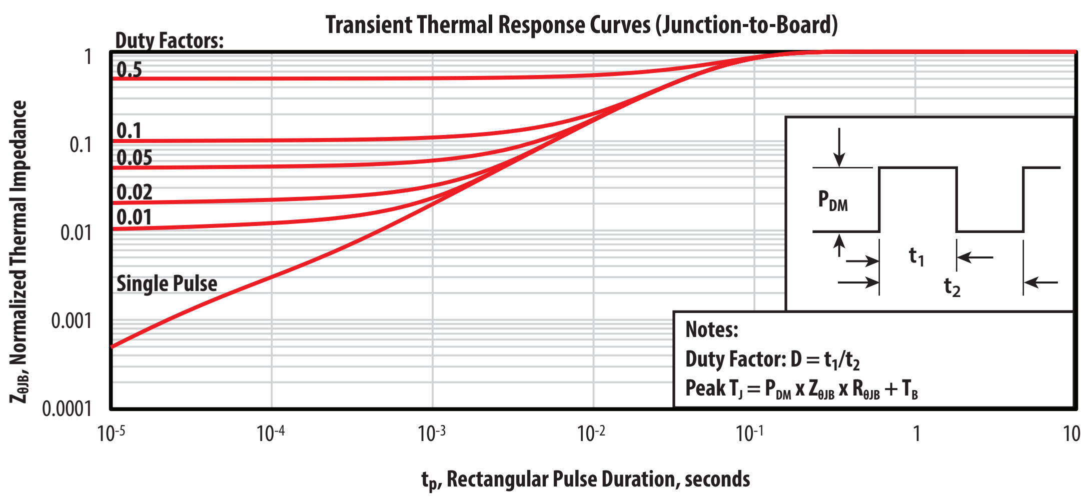


Figure 11: Transient Thermal Response Curves



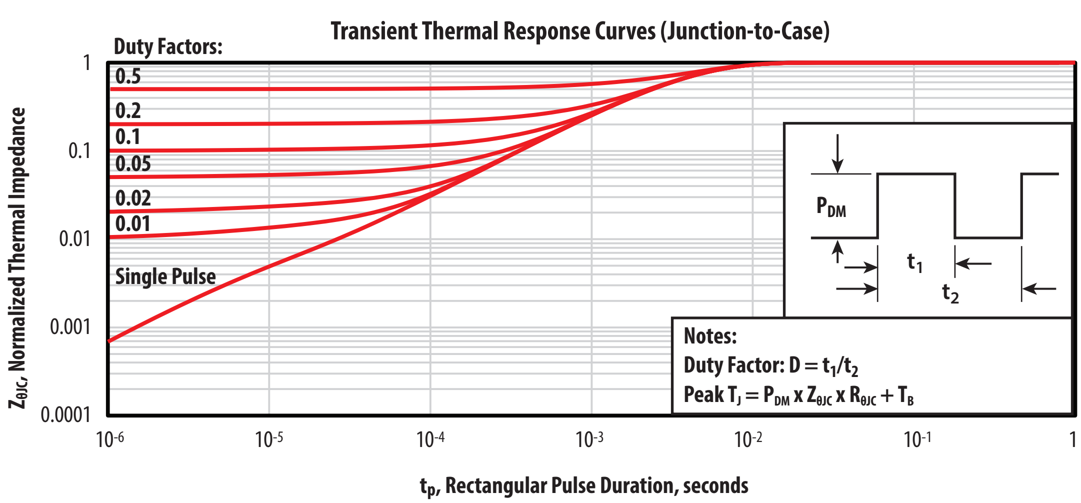
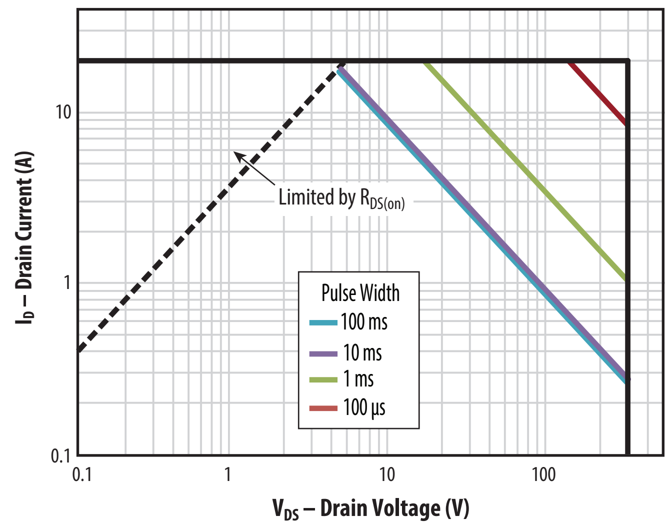
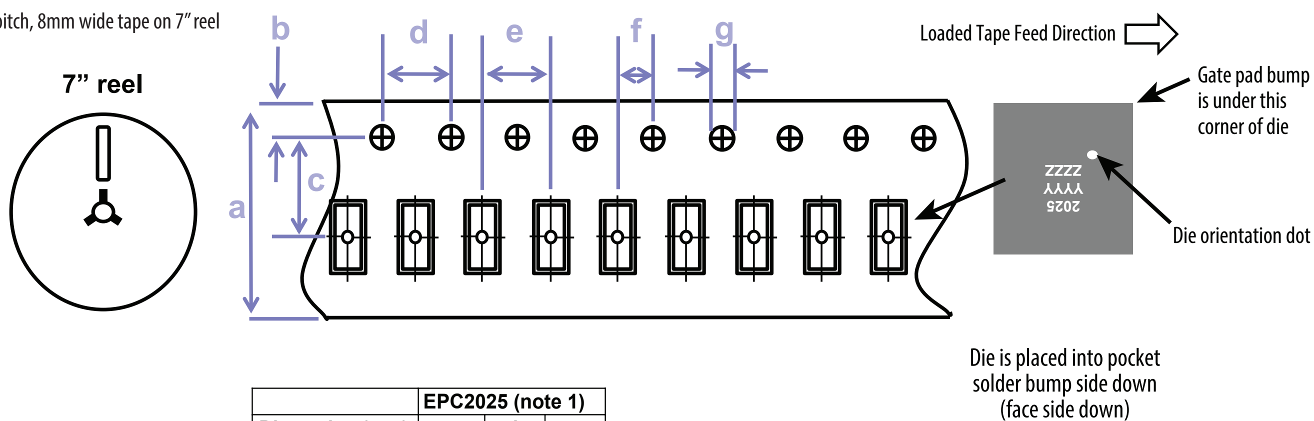


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

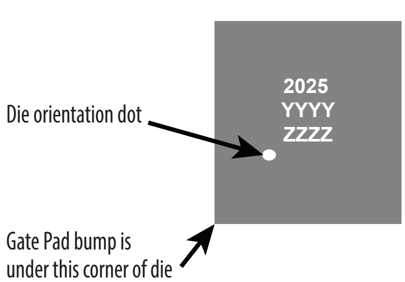
4mm pitch, 8mm wide tape on 7" reel



	EPC2025 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

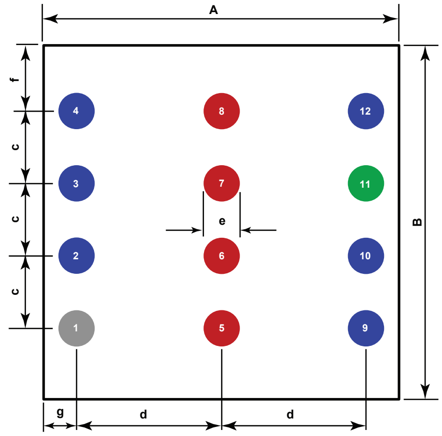
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2025	2025	YYYY	ZZZZ

DIE OUTLINE

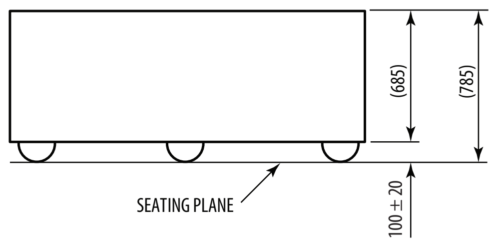
Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	1920	1950	1980
B	1920	1950	1980
c	400	400	400
d	800	800	800
e	180	200	220
f	360	375	390
g	160	175	190

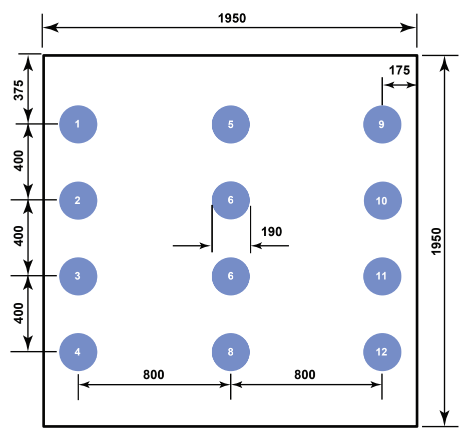
Pad 1 is Gate;
Pads 5, 6, 7, 8 are Drain;
Pads 2, 3, 4, 9, 10, 12 are Source;
Pad 11 is Substrate

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)



The land pattern is solder mask defined

Solder mask is 5 µm smaller per side than bump

Pad 1 is Gate;

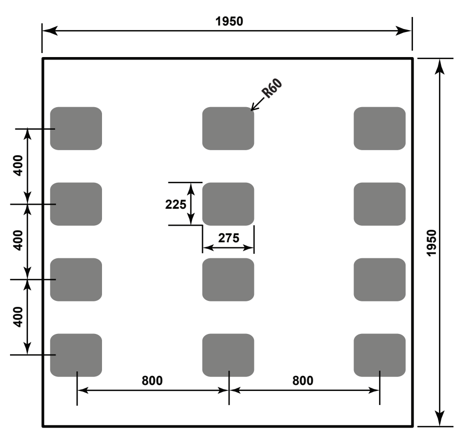
Pads 2, 3, 4, 9, 10, 12 are Source;

Pads 5, 6, 7, 8 are Drain;

Pad 11 is Substrate

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx