MC14012B

Dual 4-Input NAND Gates

The MC14012B dual 4−input NAND gates are constructed with P−Channel and N−Channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin−for−Pin Replacements for Corresponding CD4000 Series B Suffix Devices
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
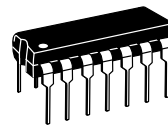
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
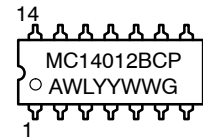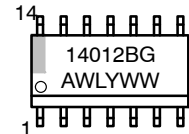
ON Semiconductor®

MARKING DIAGRAMS

PDIP−14
P SUFFIX
CASE 646

14

MC14012BCP
○ AWLYYWWG

1

SOIC−14
D SUFFIX
CASE 751A

14

14012BG
AWLYWW

1

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14012B

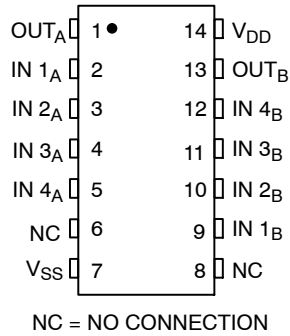## MC14012B
Dual 4−Input NAND Gate

OUT$_A$ — 1 •   14 — V$_{DD}$
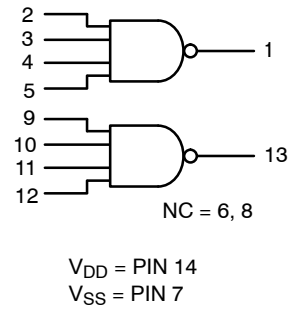IN 1$_A$ — 2   13 — OUT$_B$
IN 2$_A$ — 3   12 — IN 4$_B$
IN 3$_A$ — 4   11 — IN 3$_B$
IN 4$_A$ — 5   10 — IN 2$_B$
NC — 6   9 — IN 1$_B$
V$_{SS}$ — 7   8 — NC

NC = NO CONNECTION

Figure 1. Pin Assignment

NC = 6, 8

V$_{DD}$ = PIN 14
V$_{SS}$ = PIN 7

Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC14012BCPG	PDIP−14 (Pb−Free)	25 Units / Rail
MC14012BDG	SOIC−14 (Pb−Free)	55 Units / Rail
MC14012BDR2G	SOIC−14 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current ($V_{OH} = 2.5$ Vdc) Source	I_{OH}	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
($V_{OH} = 4.6$ Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
($V_{OH} = 9.5$ Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
($V_{OH} = 13.5$ Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
($V_{OL} = 0.4$ Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
($V_{OL} = 0.5$ Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
($V_{OL} = 1.5$ Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	μAdc
Input Capacitance ($V_{in} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.5	–	0.0010	0.5	–	15	
		15	–	1.0	–	0.0015	1.0	–	30	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Gate, $C_L = 50$ pF)	I_T	5.0	$I_T = (0.3 \text{ μA/kHz}) f + I_{DD}/N$							μAdc
		10	$I_T = (0.6 \text{ μA/kHz}) f + I_{DD}/N$							
		15	$I_T = (0.9 \text{ μA/kHz}) f + I_{DD}/N$							

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
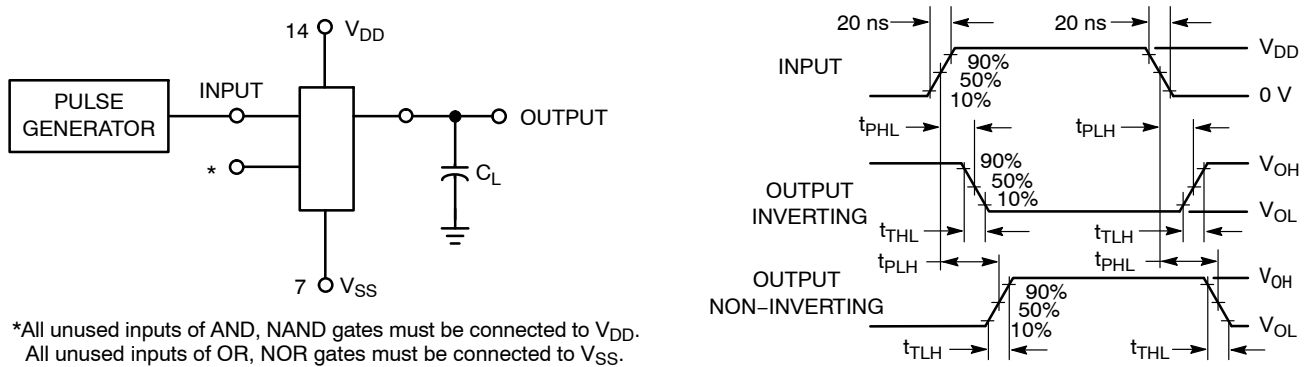3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \, Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001$ x the number of exercised gates per package.

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SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time t_{TLH} = (1.35 ns/pF) C_L + 33 ns t_{TLH} = (0.60 ns/pF) C_L + 20 ns t_{TLH} = (0.40 ns/PF) C_L + 20 ns	t_{TLH}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Output Fall Time t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{THL} = (0.40 ns/pF) C_L + 20 ns	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	160 65 50	300 130 100	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

Figure 3. Switching Time Test Circuit and Waveforms

*Inverter omitted
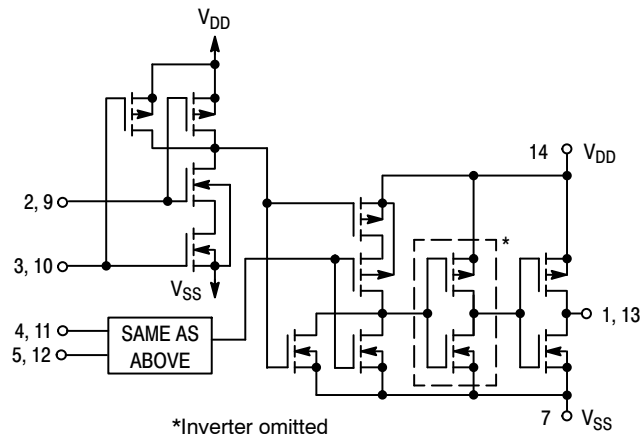
Figure 4. Circuit Schematic – One of Two Gates Shown

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TYPICAL B–SERIES GATE CHARACTERISTICS

N–CHANNEL DRAIN CURRENT (SINK)

Figure 5. V$_{GS}$ = 5.0 Vdc

P–CHANNEL DRAIN CURRENT (SOURCE)
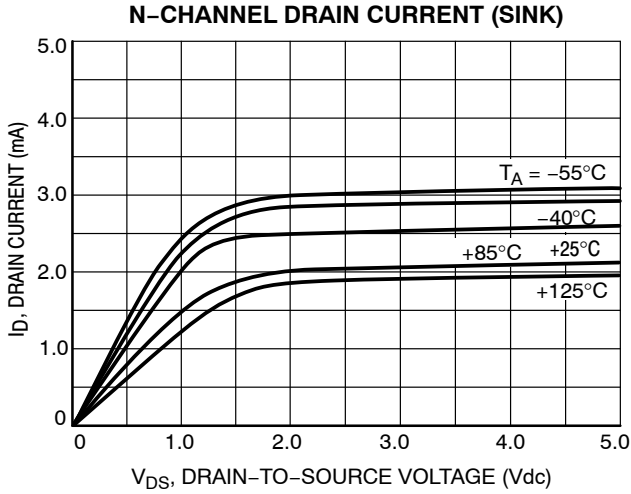
Figure 6. V$_{GS}$ = − 5.0 Vdc

Figure 7. V$_{GS}$ = 10 Vdc
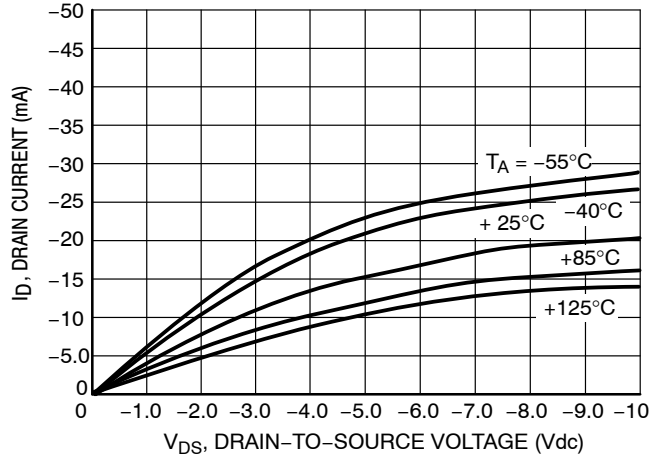
Figure 8. V$_{GS}$ = − 10 Vdc
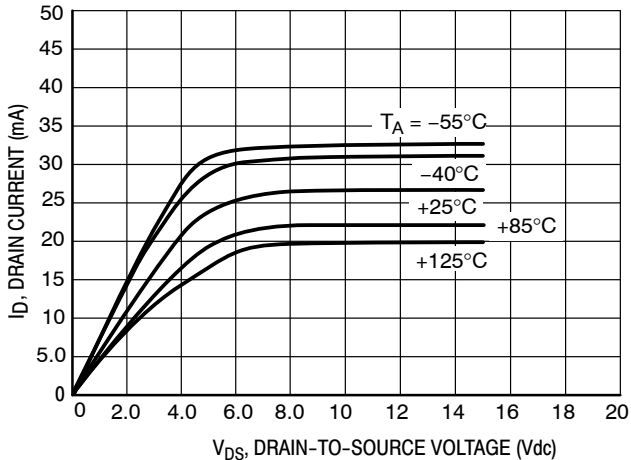
Figure 9. V$_{GS}$ = 15 Vdc
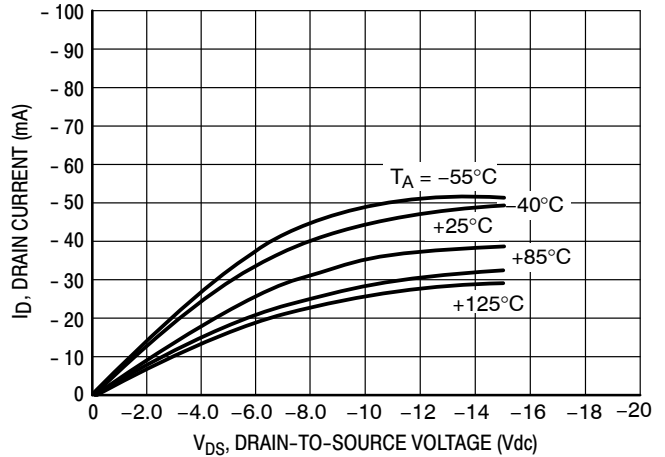
Figure 10. V$_{GS}$ = − 15 Vdc

These typical curves are not guarantees, but are design aids.
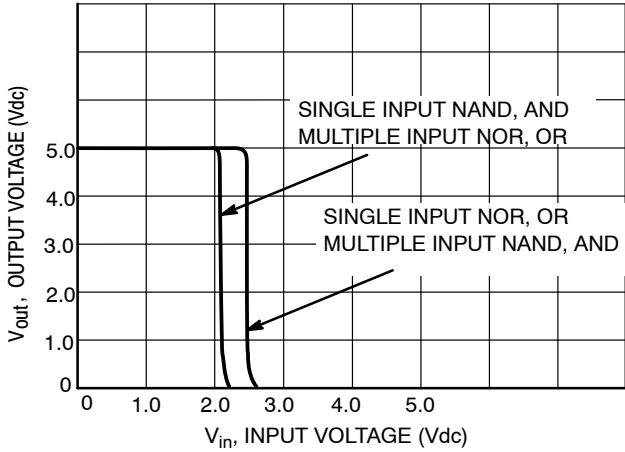Caution: The maximum rating for output current is 10 mA per pin.

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VOLTAGE TRANSFER CHARACTERISTICS

Figure 11. V$_{DD}$ = 5.0 Vdc
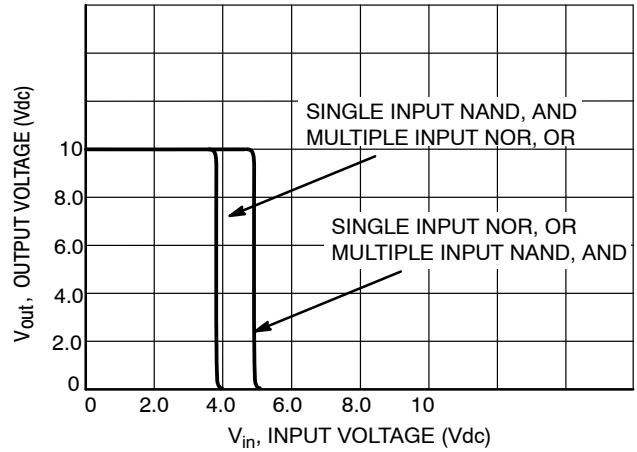
Figure 12. V$_{DD}$ = 10 Vdc
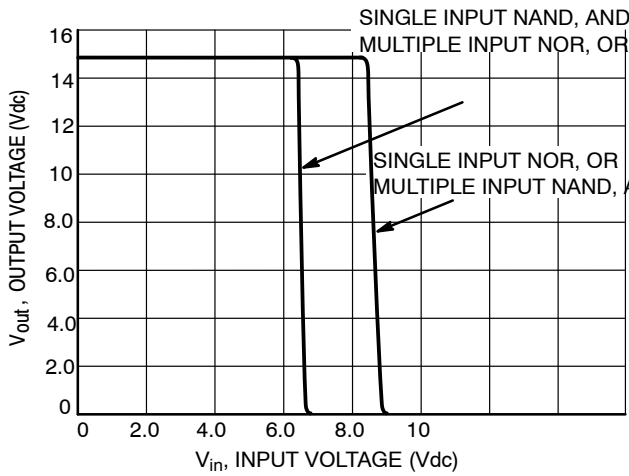
Figure 13. V$_{DD}$ = 15 Vdc

DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V$_{IL}$ and V$_{IH}$ for the output(s) to be at a fixed voltage V$_O$ are given in the Electrical Characteristics table. V$_{IL}$ and V$_{IH}$ are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

   1.0 V with a 5.0 V supply
   2.0 V with a 10.0 V supply
   2.5 V with a 15.0 V supply
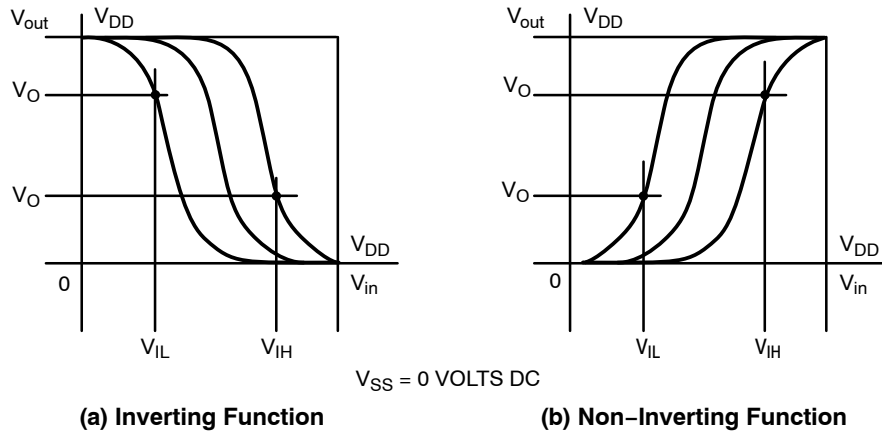
(a) Inverting Function

(b) Non−Inverting Function

V$_{SS}$ = 0 VOLTS DC

Figure 14. DC Noise Immunity

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PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P
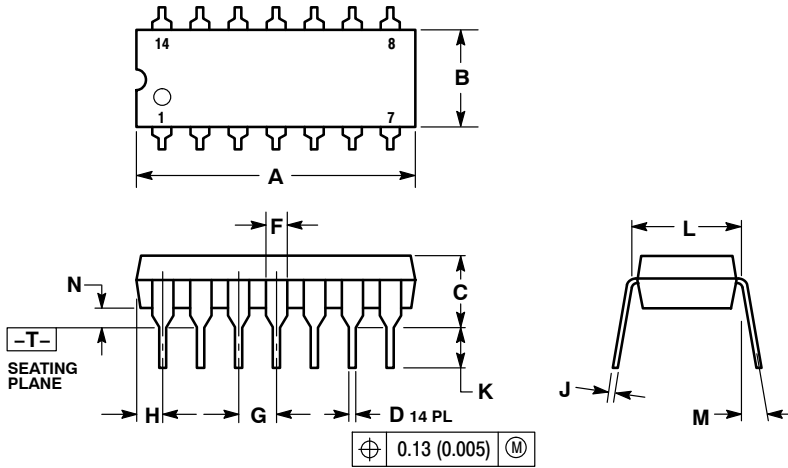
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 °	−−−	10 °
N	0.015	0.039	0.38	1.01

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PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE K
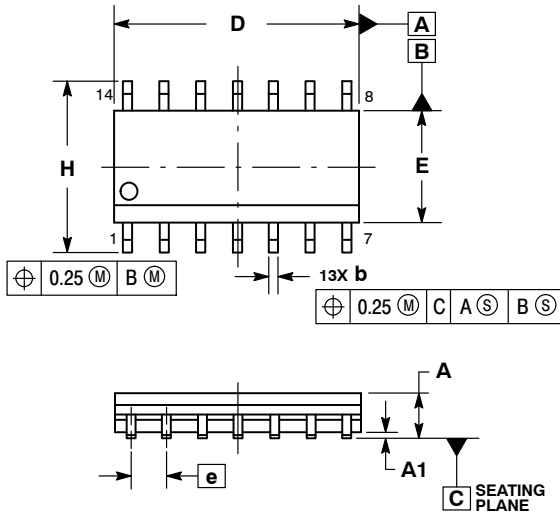
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

DETAIL A

SEATING PLANE

SOLDERING FOOTPRINT*

6.50

14X 1.18

1

1.27 PITCH

14X 0.58
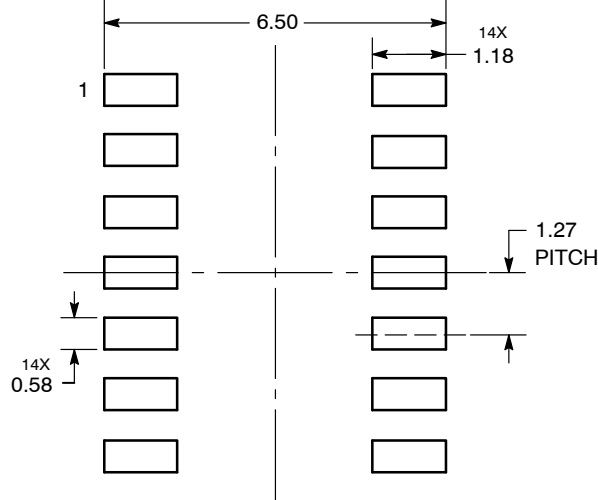
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14012B/D