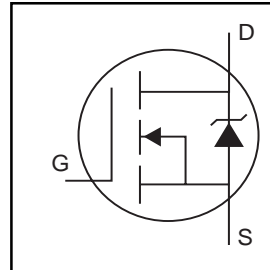


- Logic-Level Gate Drive
- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated

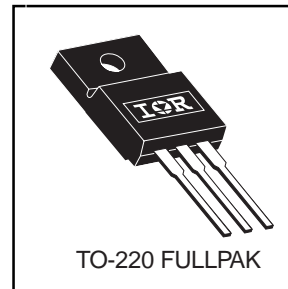


$V_{DS} = 100V$
$R_{DS(on)} = 0.18\Omega$
$I_D = 8.1A$

**Description**

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



TO-220 FULLPAK

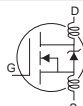
**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	8.1	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5.7	
$I_{DM}$	Pulsed Drain Current ①⑥	35	
$P_D @ T_C = 25^\circ C$	Power Dissipation	30	W
	Linear Derating Factor	0.20	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy②⑥	85	mJ
$I_{AR}$	Avalanche Current①⑥	6.0	A
$E_{AR}$	Repetitive Avalanche Energy①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	5.0	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	5.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	65	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA <sup>⑥</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.18	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6.0A <sup>④</sup>
		—	—	0.22		V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 6.0A <sup>④</sup>
		—	—	0.26		V <sub>GS</sub> = 4.0V, I <sub>D</sub> = 5.0A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	3.1	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 6.0A <sup>⑥</sup>
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -16V
Q <sub>g</sub>	Total Gate Charge	—	—	20	nC	I <sub>D</sub> = 6.0A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	4.6		V <sub>DS</sub> = 80V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	10		V <sub>GS</sub> = 5.0V, See Fig. 6 and 13 <sup>④⑥</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	40	—	ns	V <sub>DD</sub> = 50V
t <sub>r</sub>	Rise Time	—	35	—		I <sub>D</sub> = 6.0A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	23	—		R <sub>G</sub> = 11Ω, V <sub>GS</sub> = 5.0V
t <sub>f</sub>	Fall Time	—	22	—		R <sub>D</sub> = 8.2Ω, See Fig. 10 <sup>④⑥</sup>
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	440	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	97	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	50	—		f = 1.0MHz, See Fig. 5 <sup>⑥</sup>
C	Drain to Sink Capacitance	—	12	—		f = 1.0MHz

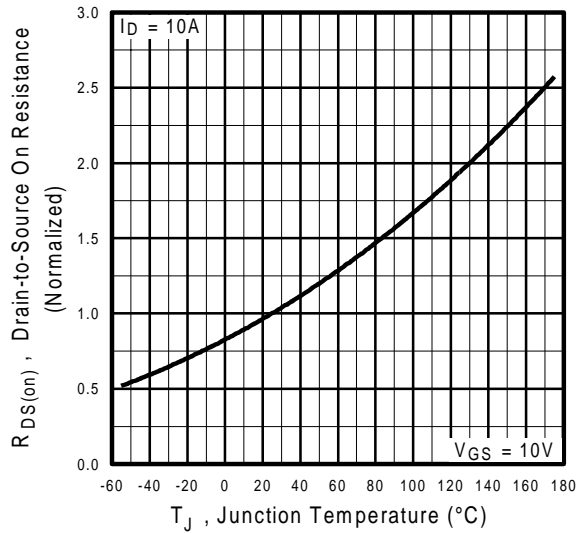
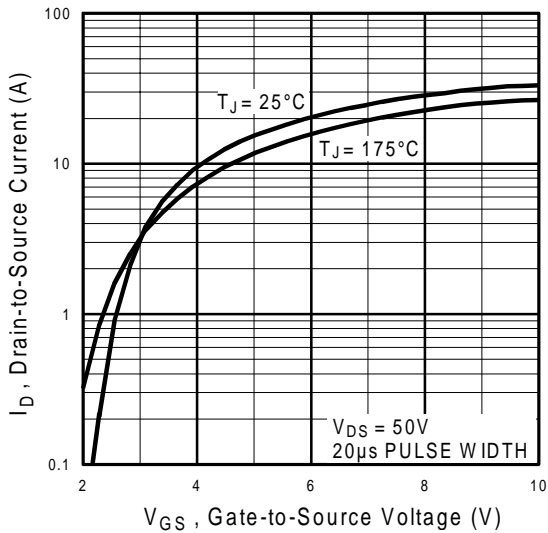
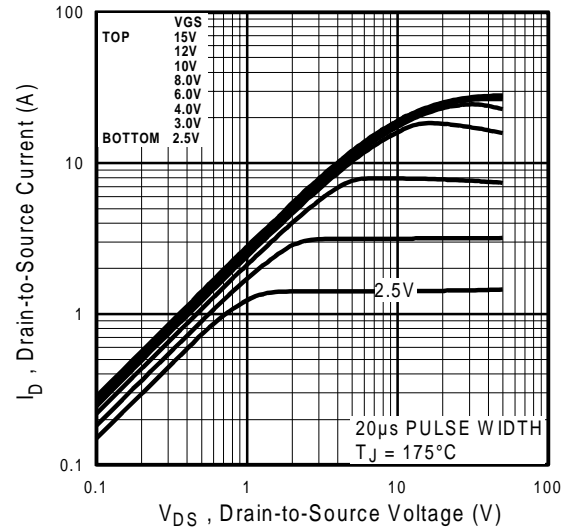
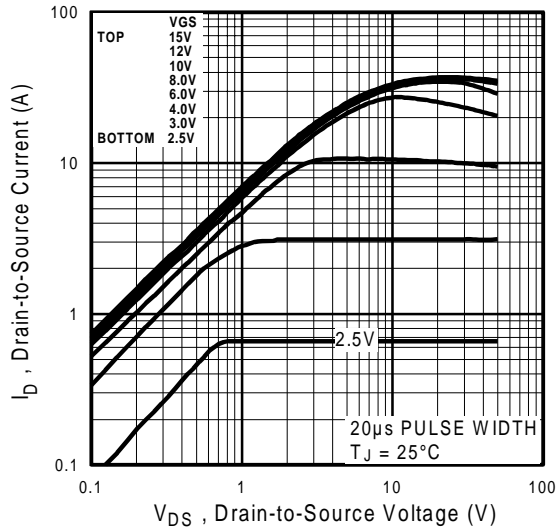
## Source-Drain Ratings and Characteristics

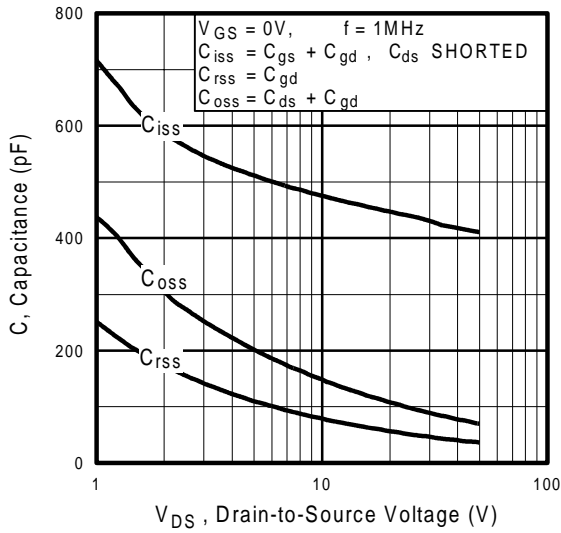
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	8.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①⑥</sup>	—	—	35		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 6.0A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	110	160	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 6.0A
Q <sub>rr</sub>	Reverse Recovery Charge	—	410	620	nC	di/dt = 100A/μs <sup>④⑥</sup>
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

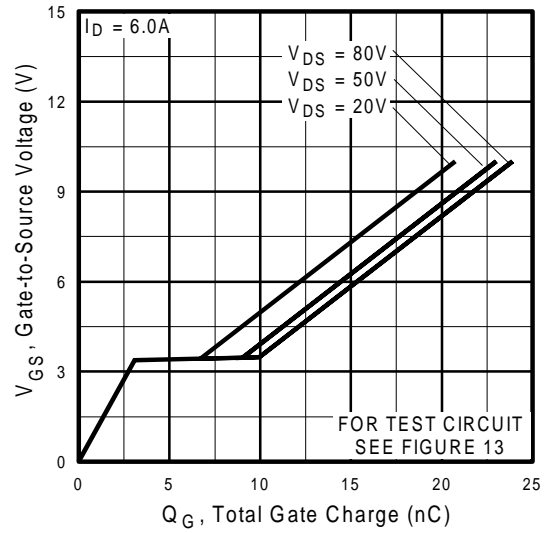
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting T<sub>J</sub> = 25°C, L = 4.7mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 6.0A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ 6.0A, di/dt ≤ 340A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C

- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ t = 60s, f = 60Hz
- ⑥ Uses IRL520N data and test conditions

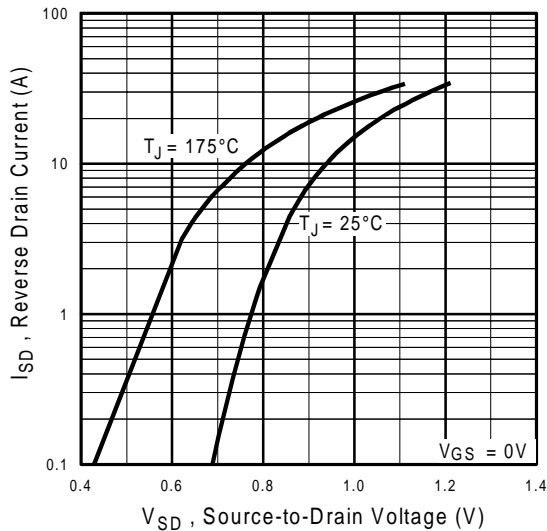




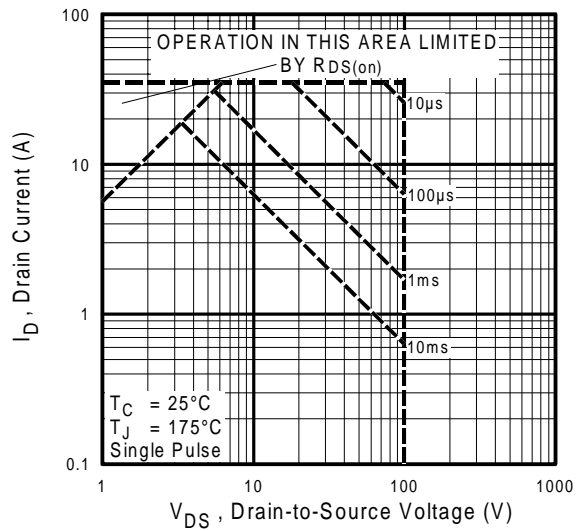
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



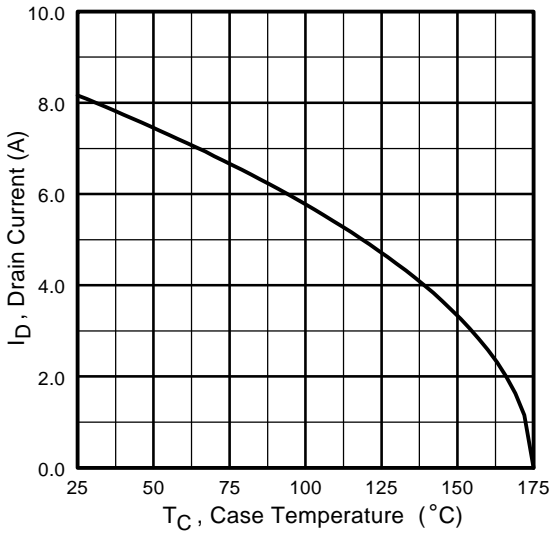
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



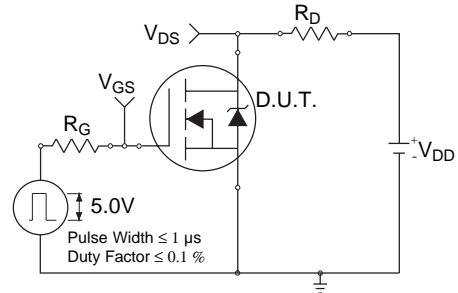
**Fig 7.** Typical Source-Drain Diode Forward Voltage



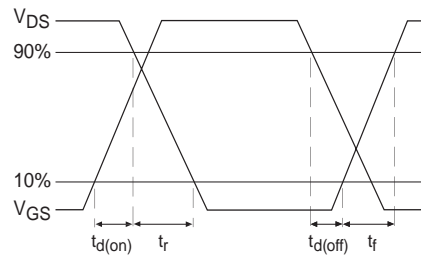
**Fig 8.** Maximum Safe Operating Area



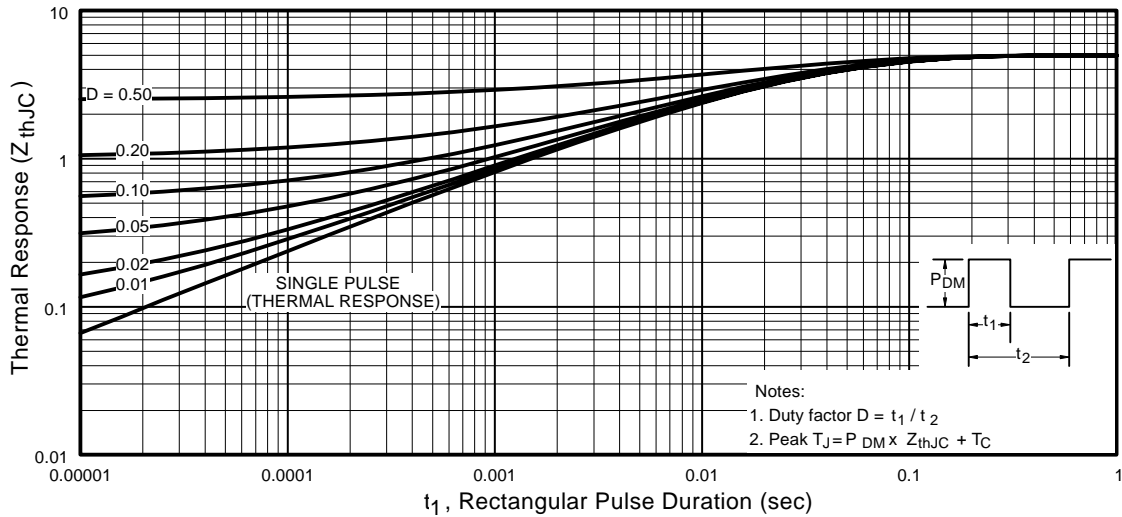
**Fig 9.** Maximum Drain Current Vs. Case Temperature



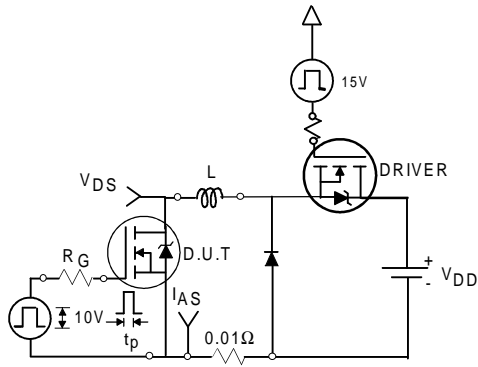
**Fig 10a.** Switching Time Test Circuit



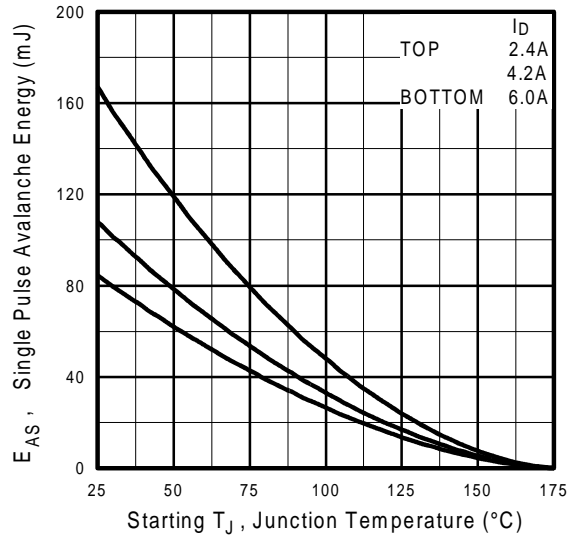
**Fig 10b.** Switching Time Waveforms



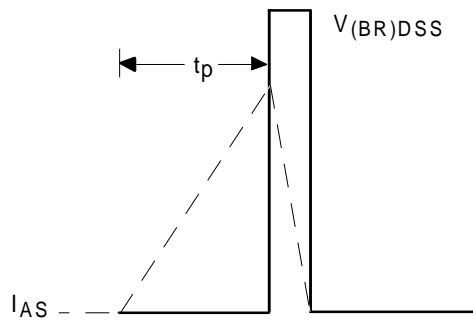
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



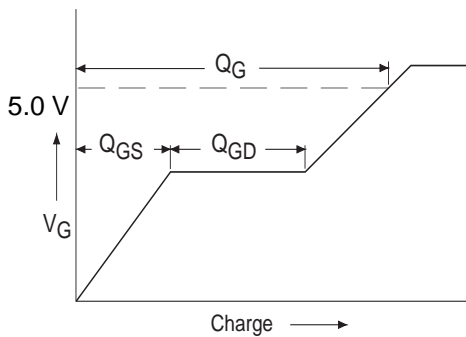
**Fig 12a.** Unclamped Inductive Test Circuit



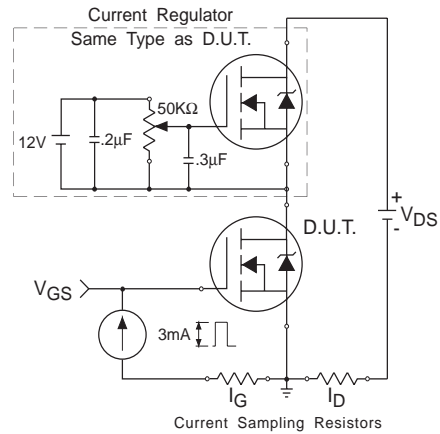
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12b.** Unclamped Inductive Waveforms

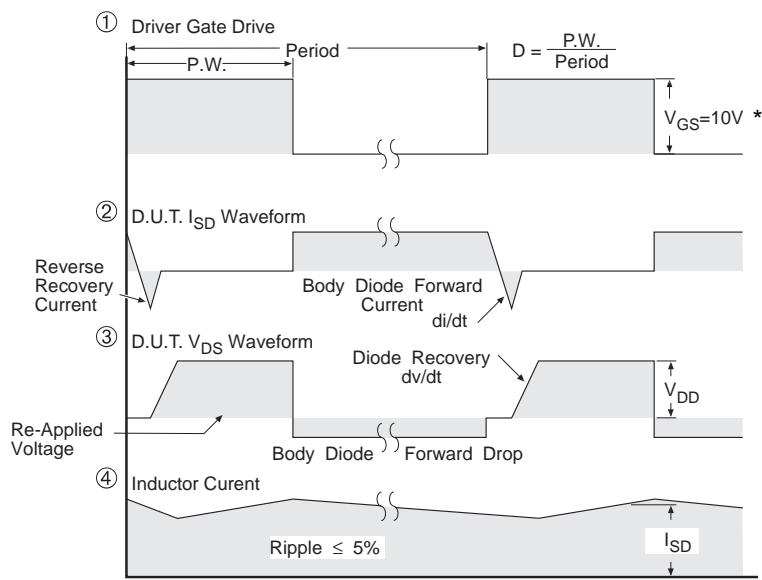
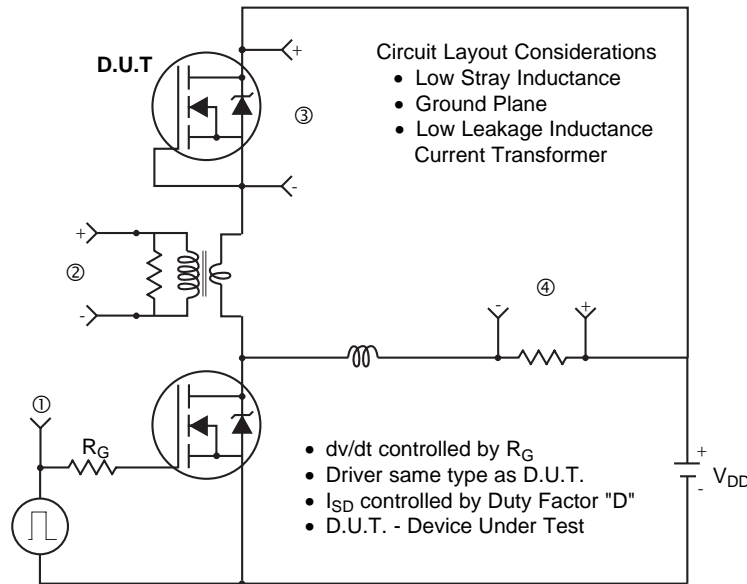


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

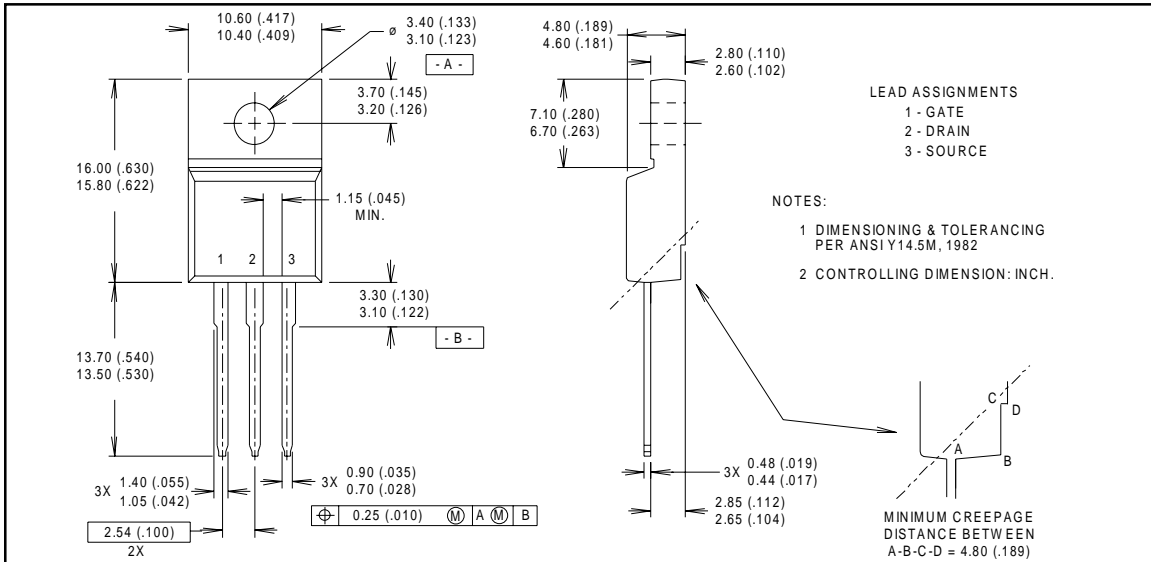
# IRLI520N

International  
**IR** Rectifier

## Package Outline

### TO-220 Fullpak Outline

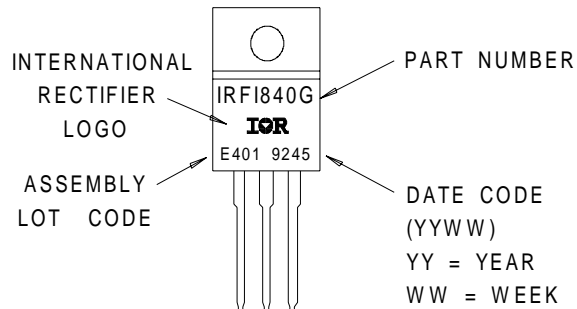
Dimensions are shown in millimeters (inches)



## Part Marking Information

### TO-220 Fullpak

EXAMPLE : THIS IS AN IRFI840G  
WITH ASSEMBLY  
LOT CODE E401



International  
**IR** Rectifier

**WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331  
**EUROPEAN HEADQUARTERS:** Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

**IR CANADA:** 15 Lincoln Court, Brampton, Ontario L6T 3Z2, Tel: (905) 453 2200

**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

**IR FAR EAST:** 171 (K&H Bldg.) 30-4 Nishi-ikebukuro 3-chome, Toshima-ku, Tokyo Japan Tel: 81 33 983 0086

**IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 16907 Tel: 65 221 8371

*Data and specifications subject to change without notice.*

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>