PIC18F2420/2520/4420/4520 Rev. B2 Silicon Errata

The PIC18F2420/2520/4420/4520 Rev. B2 parts you have received conform functionally to the Device Data Sheet (DS39631**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2420/2520/4420/4520 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2420/2520/4420/4520 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2420	0001 0001 010	0 0101
PIC18F2520	0001 0001 000	0 0101
PIC18F4420	0001 0000 110	0 0101
PIC18F4520	0001 0000 100	0 0101

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

1. Module: MSSP

In SPI Slave mode with slave select enabled (SSPM<3:0> = 0100), the minimum time between the falling edge of the $\overline{SS}$ pin and first SCK edge is greater than specified in parameter 70 in Table 26-16 and Table 26-17. The updated specification is shown in bold in Table 1.

The minimum time between the $\overline{SS}$ pin low and an SSPBUF write is also 3 TCY. If the falling edge of the $\overline{SS}$ pin occurs greater than 3 TCY before the first SCK edge, or loading SSPBUF, the peripheral will function correctly. Also, if SSPBUF is written prior to the $\overline{SS}$ pin going low, the peripheral will function correctly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input	**3 TCY**	—	ns	

2. Module: MSSP

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate, and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur, as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Timer1 and Timer3

For Timer1 or Timer3, if the TMRxH and TMRxL registers are written to in consecutive instruction cycles, the timer may not be updated with the correct value when configured for externally clocked 8-Bit Asynchronous mode (T1CON<7:0> or T3CON<7:0> = 0xxx x111).

Work around

Insert a delay of one or more instruction cycles between writes to TMRxH and TMRxL. This delay can be a NOP, or any instruction that does not access the Timer registers (Example 1).

EXAMPLE 1:

```
CLRF    TMR1H
MOVLW   T1Offset  ; 1 Tcy delay
MOVWF   TMR1L
```

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: ECCP (PWM Mode)

Note: The ECCP module is implemented only in 40/44-pin devices.

When configured for half-bridge operation with dead band (CCPxCON<7:6> = 10), the PWM output may be corrupted for certain values of the PWM duty cycle. This occurs when these additional criteria are also met:

- a non-zero, dead-band delay is specified (PDC6:PDC0 > 0); and
- the duty cycle has a value of 0 through 3, or 4n + 3 (n ≥ 1).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Power-up Timer

The Power-up Timer (PWRT) may not function as expected during a Power-on Reset (POR) when the Brown-out Reset (BOR) is disabled.

Work around

Use either of the following work arounds:

- Enable the BOR using any desired mode and setpoint.
- If BOR operation is not desired:
  - Configure the BOR using BOREN<1:0> = 01 (CONFIG2L<2:1>) – BOR controlled by SBOREN.
  - Configure the BOR for the lowest voltage setpoint by clearing the BORV<1:0> bits (CONFIG2L<4:3>).

  In this configuration, the SBOREN bit resets to '1', enabling the BOR.
  - When code execution begins following all Resets, disable the BOR by clearing the SBOREN bit (RCON<6>).

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

One bit has been added to the BAUDCON register and one bit has been renamed. The added bit is RXDTP and is in the location, BAUDCON<5>. The renamed bit is the TXCKP bit (BAUDCON<4>), which had been named SCKP.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the Synchronous mode TX and RX signals to be inverted (polarity reversed). RXDTP has no effect on the Synchronous mode DT signal.

Register 18-3, on page 204, will be changed as shown.

Work around

None required.

Date Codes that pertain to this issue:

All engineering and production devices.

REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is Active

bit 5 **RXDTP**: Receive Data Polarity Select bit (Asynchronous mode only)
Asynchronous mode:
1 = Receive data (RX) is inverted. Idle state is a low level.
0 = No inversion of receive data (RX). Idle state is a high level.

bit 4 **TXCKP**: Transmit/Clock Polarity Select bit
Asynchronous mode:
1 = Transmit data (TX) is inverted. Idle state is a low level.
0 = No inversion of transmit data (TX). Idle state is a high level.
Synchronous mode:
1 = Idle state for clock (CK) is a high level
0 = Idle state for clock (CK) is a low level

bit 3 **BRG16:** 16-bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode); SPBRGH value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RX pin with the interrupt generated on the falling edge; bit cleared in hardware on following rising edge
0 = RX pin is not monitored or rising edge detected
Synchronous mode:
Unused in this mode.

REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER (CONTINUED)

bit 0 **ABDEN**: Auto-Baud Detect Enable bit

Asynchronous mode:

1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.

0 = Baud rate measurement disabled or completed

Synchronous mode:

Unused in this mode.

7. Module: 10-Bit Analog-to-Digital Converter

When the AD clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select the AD clock source as 4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC and avoid selecting 2 TOSC or RC.

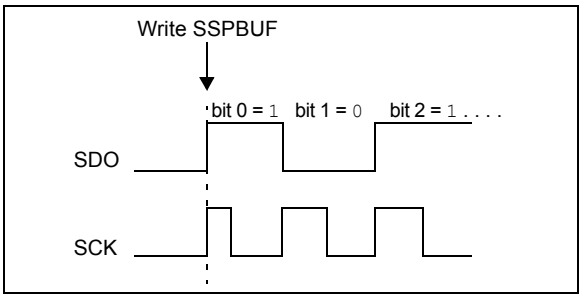
Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 2 for sample code.

EXAMPLE 2: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSS  SSPSTAT, BF     ;Data received?
                            ;(Xmit complete?)
     BRA    LOOP            ;No
     MOVF   SSPBUF, W       ;W = SSPBUF
     MOVWF  RXDATA          ;Save in user RAM
     MOVF   TXDATA, W       ;W = TXDATA
     BCF    T2CON, TMR2ON   ;Timer2 off
     CLRF   TMR2            ;Clear Timer2
     MOVWF  SSPBUF          ;Xmit New data
     BSF    T2CON, TMR2ON   ;Timer2 on
```

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (08/2006)
First revision of this document. Silicon issues 1-2 (MSSP).

Rev B Document (10/2006)
Added silicon issue 3 (Timer1 and Timer3).

Rev C Document (11/2006)
Updated silicon issue 3 (Timer1 and Timer3) and added silicon issue 4 (ECCP – PWM Mode).

Rev D Document (1/2007)
Added silicon issue 5 (Power-up Timer).

Rev E Document (4/2007)
Added silicon issue 6 (Enhanced Universal Synchronous Receiver Transmitter – EUSART).

Rev F Document (6/2007)
Added silicon issue 7 (10-Bit Analog-to-Digital Converter) and 8 (MSSP – SPI Mode).

Rev G Document (8/2007)
Modified silicon issue 6 (EUSART).

NOTES:

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