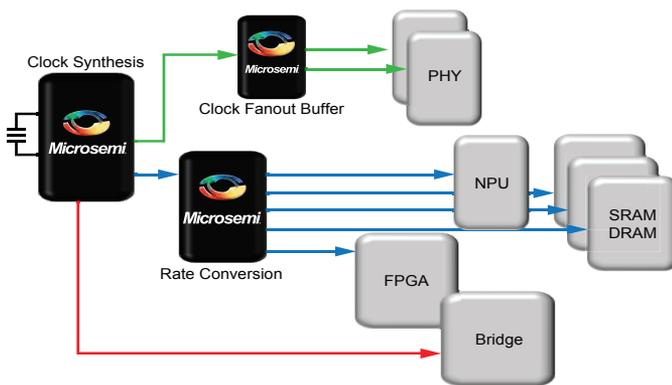


Rate Conversion/Jitter Attenuation Products

System clock trees are becoming more complex often requiring rate conversion with jitter attenuation at very low bandwidth frequencies and distribution of several clock frequencies to multiple loads. Rate conversion/jitter attenuation devices from Microsemi® can lock to input clock signals and filter jitter starting at 30 mHz. These devices lower bill of material costs, simplify design, and improve performance by replacing external components traditionally used to build timing clock trees with a fully integrated single chip-solution.



Applications

- Timing generation for enterprise routers and switches, storage area network equipment, servers, communications equipment, and broadcast video applications
- Processor, processor bus, SDRAM, and DDR clocks
- Timing for 10 Gigabit CDRs, Rapid-I/O, PCIe, Serial MI, Star Fabric, Fibre Channel, XAUI

Availability and Support

Microsemi Clock Management products are in volume production. To learn more about Microsemi's clock products, visit www.microsemi.com/products/timing-and-synchronization/frequency-conversion. Full information, including complete data sheets and design manuals, is available to registered MyMicrosemi customers. To register for a MyMicrosemi account, visit www.microsemi.com/create-an-account.

Clock Rate Conversion Solutions Address Key Customer Pains

- Providing spec-compliant timing for multi-gigabit PHYs is difficult
- Adding external jitter cleaning circuitry to provide PHYs with spec-compliant timing is costly and complex

High Integration

- Up to 2 independent programmable synthesizers replace competing multi-chip single channel solutions
- Integrated fanout buffers with up to 20 output clock signals in two frequency families

Industry Leading Ultra-low Jitter

- Ultra – low 160 fs jitter on all outputs
- Low bandwidth jitter filtering on input clock signals starting at 30 mHz

Wide Frequency Range

- Output clock frequencies from <1 Hz to 1035 MHz
- Fractional synthesizers support any-to-any clock synthesis

Highly Programmable Outputs

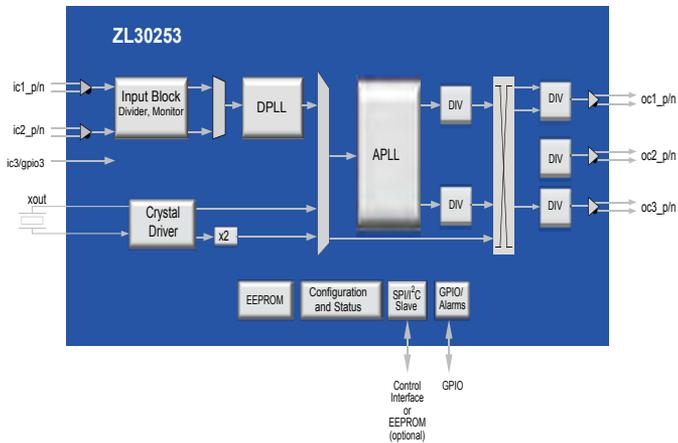
- Control of each output clock's signal format, voltage, drive strength, frequency divider, and phase
- Replace external support components such as fanout buffers and format converters

Custom Configuration

- Clock signals available at power-up with integrated EEPROM; easily configurable with hardware pins

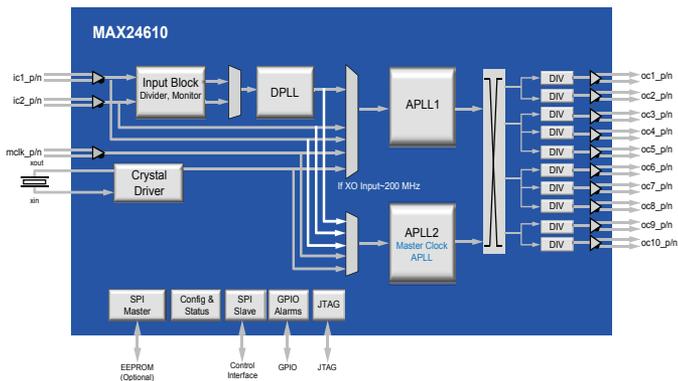
Rate Conversion/Jitter Attenuation Products

Featured Products



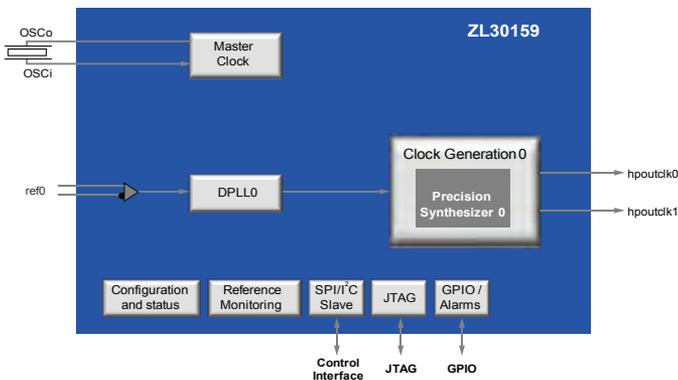
ZL30252, ZL30253, and ZL30254

- Ultra-low jitter provides spec-compliant timing for multi-gigabit interfaces
 - Any-to-any frequency conversion / jitter attenuation. Output frequencies from <1 Hz to 1035 MHz with ultra – low 160 fs RMS jitter
- Low-bandwidth DPLL
 - 14 Hz to 500 Hz programmable bandwidth, attenuates low frequency jitter
- Universal Outputs
 - Up to 6 output clock signals
 - Control over each output clock's signal format, voltage, and drive strength
 - Frequency divider and phase adjustment per output
- Numerically Controlled Oscillator mode
- Spread Spectrum mode PCIe® compliant
- Small 5mm x 5mm QFN



MAX24605 and MAX24610

- Ultra-low jitter provides spec-compliant timing for multi-gigabit interfaces
 - Any-to-any frequency conversion / jitter attenuation. Output frequencies from <1Hz to 750 MHz with ultra – low 180 fs RMS jitter
- Low-bandwidth DPLL
 - 4 Hz to 400 Hz programmable bandwidth, attenuates low frequency jitter
- On-chip fanout buffers with flexible output configuration
 - Up to 20 output clock signals in two frequency families
 - Control over each output clock's signal format, voltage, and drive strength
 - Frequency divider and phase adjustment per output
- 10mm x 10mm CSBGA



ZL30159

- Precision synthesizer generates any clock rate from 1 Hz to 177.5 MHz with jitter below 1ps
- Programmable digital PLL synchronizes to any clock rate from 1 Hz to 750 MHz Flexible output configuration
 - 30 mHz to 896 Hz programmable bandwidth, attenuates low frequency jitter
- Two LVCMOS outputs
- 9mm x 9mm LBGAs