

## AOD464

### N-Channel Enhancement Mode Field Effect Transistor

#### General Description

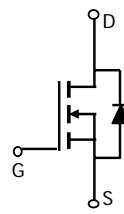
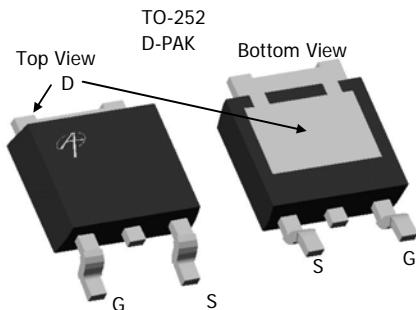
The AOD464 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in high voltage synchronous rectification, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free\*

#### Features

$V_{DS} (V) = 105V$   
 $I_D = 40 A \quad (V_{GS} = 10V)$   
 $R_{DS(ON)} < 28 m\Omega \quad (V_{GS} = 10V) @ 20A$   
 $R_{DS(ON)} < 31 m\Omega \quad (V_{GS} = 6V)$

**100% UIS Tested!**  
**100% Rg Tested!**



#### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	105	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current <sup>A</sup>	$I_D$	40	A
Current $T_C=100^\circ C$		28	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	80	
Avalanche Current <sup>C</sup>	$I_{AR}$	20	A
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	20	mJ
Power Dissipation <sup>B</sup>	$P_D$	100	W
$T_C=100^\circ C$		50	
Power Dissipation <sup>A</sup>	$P_{DSM}$	2.3	W
$T_A=70^\circ C$		1.5	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	°C

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	15	18	°C/W
Maximum Junction-to-Ambient <sup>A</sup>		45	55	°C/W
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	1	1.5	°C/W

**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D=10\text{mA}, V_{GS}=0\text{V}$	105			V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS}=84\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		1		$\mu\text{A}$
				5		
$I_{\text{GSS}}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 25\text{V}$			100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.5	3.2	4	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	80			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$		21.5	28	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		32	40	
		$V_{GS}=6\text{V}, I_D=20\text{A}$		24	31	
$g_{\text{FS}}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		50		S
$V_{\text{SD}}$	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.73	1	V
$I_S$	Maximum Body-Diode Continuous Current				55	A
<b>DYNAMIC PARAMETERS</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1\text{MHz}$		2038	2445	pF
$C_{\text{oss}}$	Output Capacitance			204		pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			85		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		1.3	1.56	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, I_D=20\text{A}$		38.5	46	nC
$Q_{\text{gs}}$	Gate Source Charge			8		nC
$Q_{\text{gd}}$	Gate Drain Charge			10		nC
$t_{\text{D(on)}}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, R_L=2.7\Omega, R_{\text{GEN}}=3\Omega$		12.7		ns
$t_r$	Turn-On Rise Time			8.2		ns
$t_{\text{D(off)}}$	Turn-Off Delay Time			31.5		ns
$t_f$	Turn-Off Fall Time			11.2		ns
$t_{\text{rr}}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}$		59.6	74	ns
$Q_{\text{rr}}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}$		161		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{\text{DSM}}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B. The power dissipation  $P_D$  is based on  $T_{J(\text{MAX})}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(\text{MAX})}=175^\circ\text{C}$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300  $\mu\text{s}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(\text{MAX})}=175^\circ\text{C}$ .

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

Rev1: Sep. 2008

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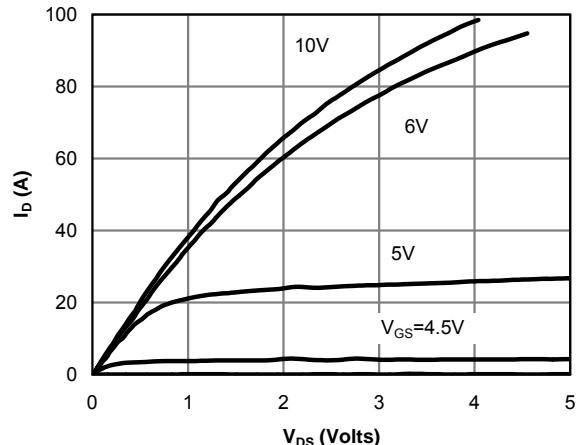
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Fig 1: On-Region Characteristics

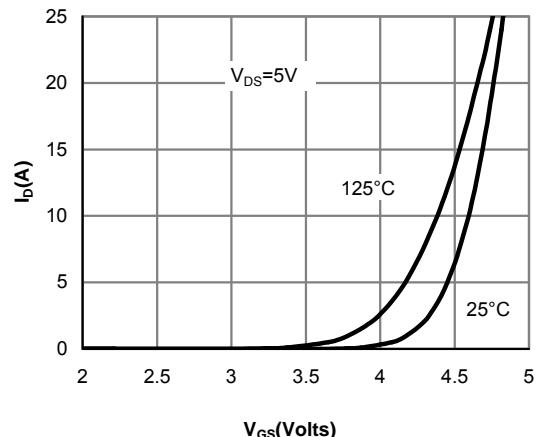


Figure 2: Transfer Characteristics

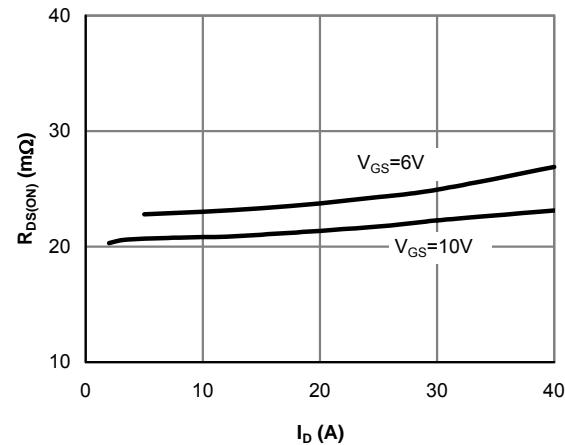


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

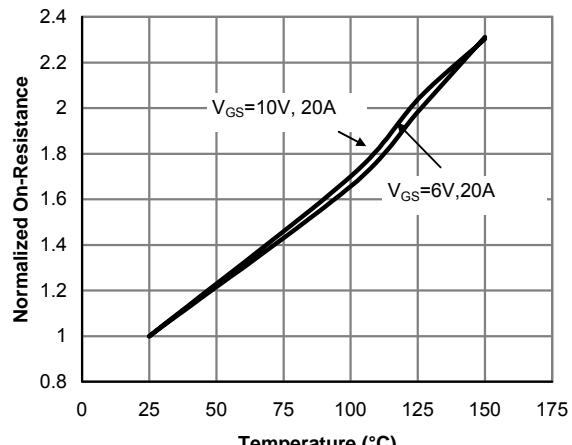


Figure 4: On-Resistance vs. Junction Temperature

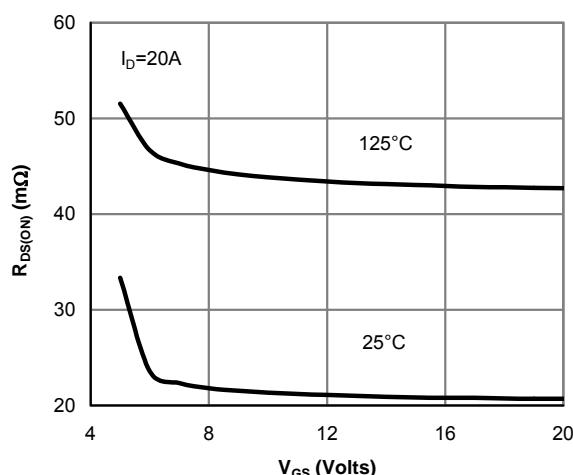


Figure 5: On-Resistance vs. Gate-Source Voltage

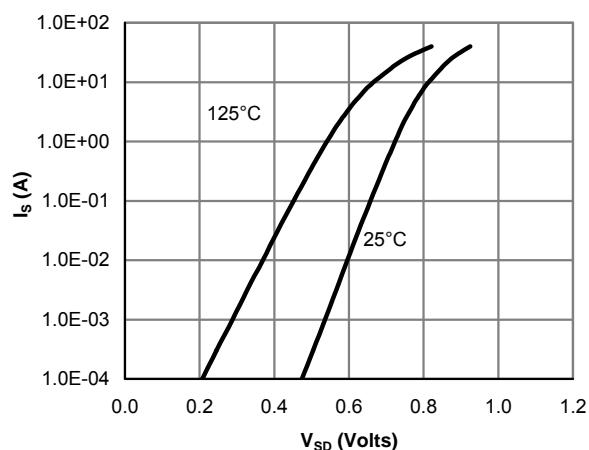


Figure 6: Body-Diode Characteristics

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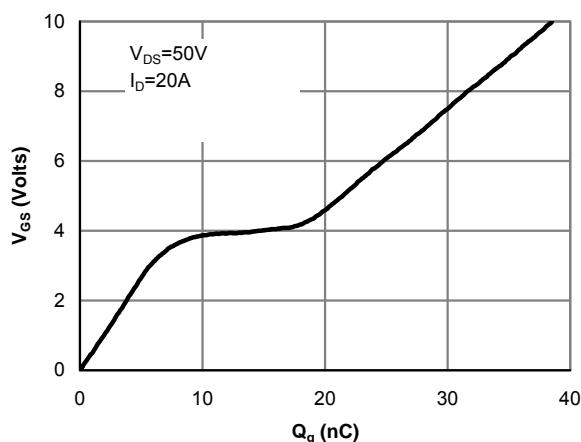
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 7: Gate-Charge Characteristics

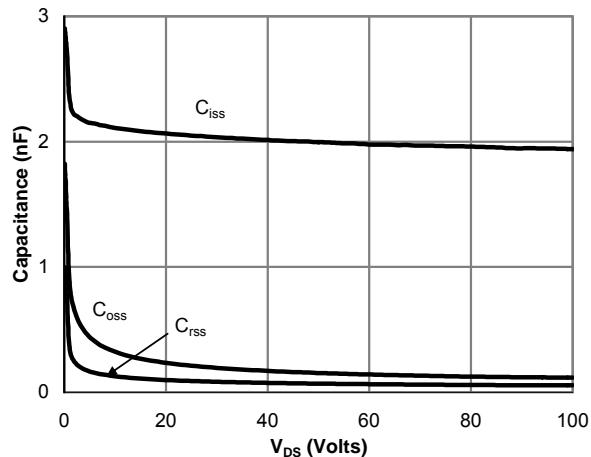


Figure 8: Capacitance Characteristics

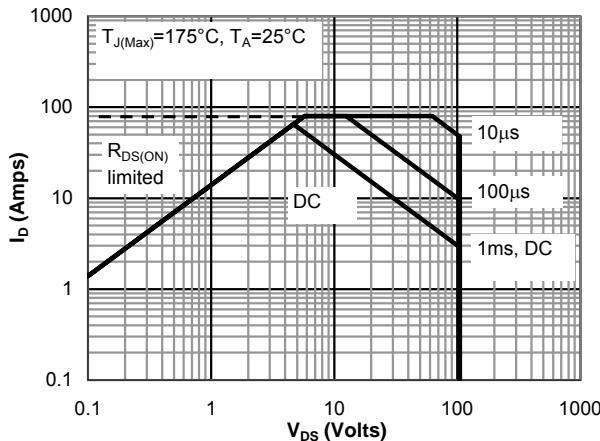


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

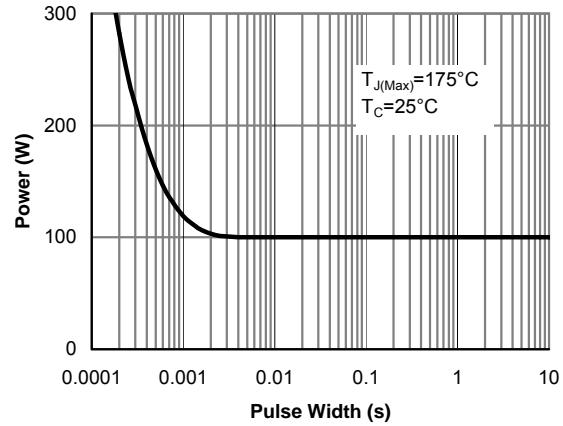


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

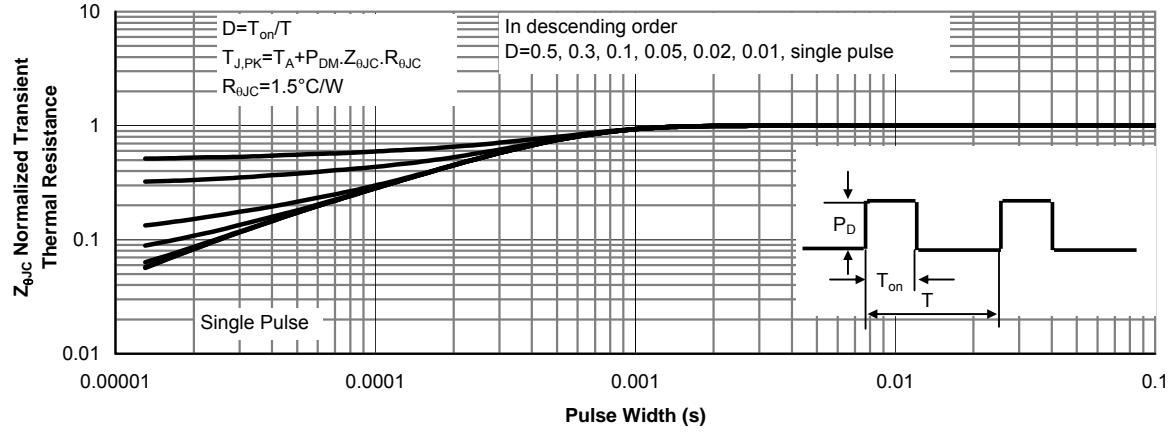


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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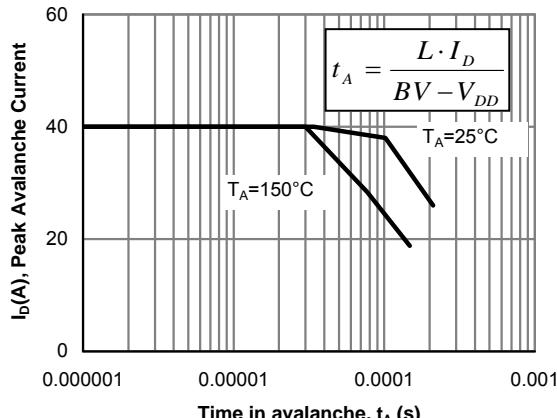
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 12: Single Pulse Avalanche capability

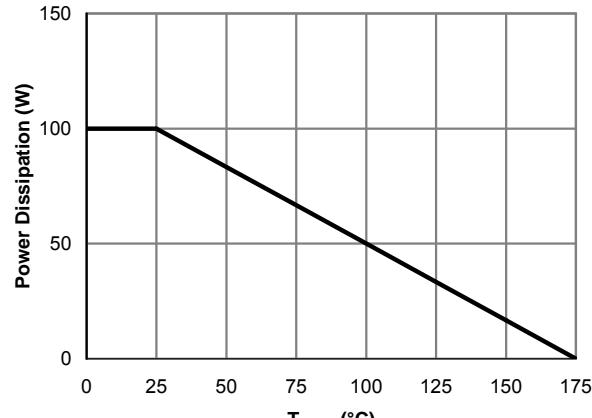


Figure 13: Power De-rating (Note B)

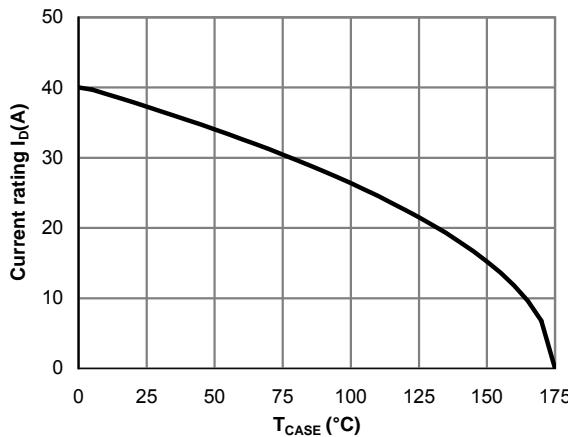


Figure 14: Current De-rating (Note B)

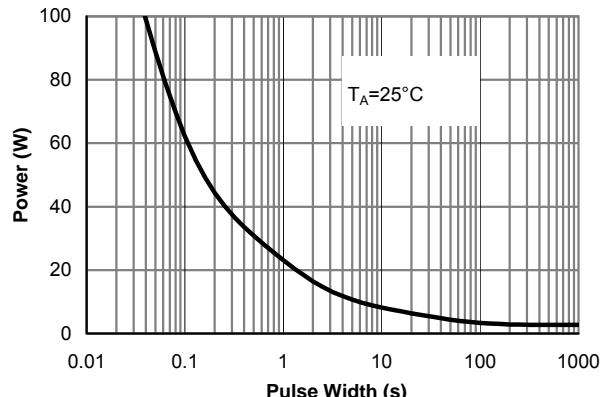


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

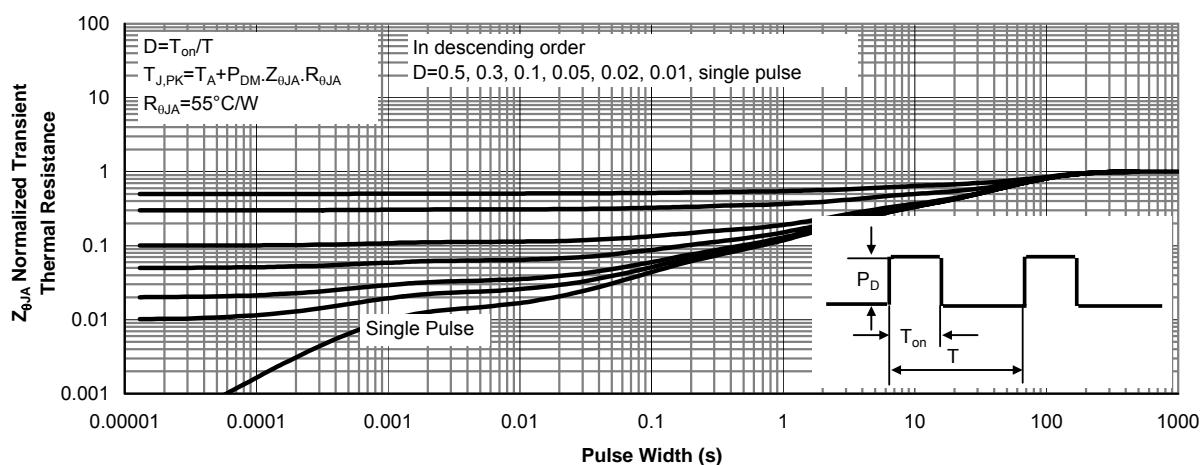
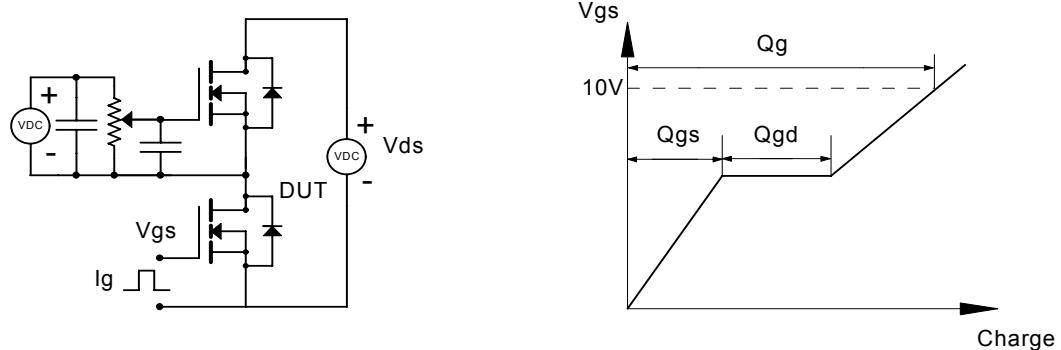
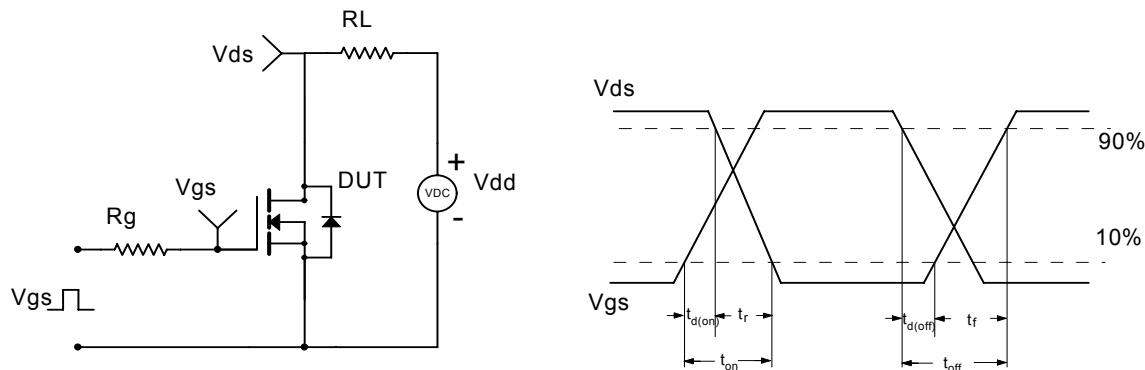


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

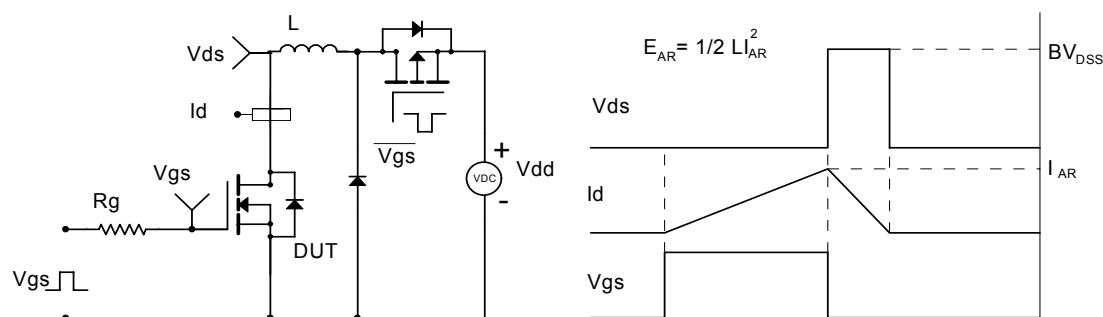
## Gate Charge Test Circuit &amp; Waveform



## Resistive Switching Test Circuit &amp; Waveforms



## Unclamped Inductive Switching (UIS) Test Circuit &amp; Waveforms



## Diode Recovery Test Circuit &amp; Waveforms

