Si5365

PIN-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

Features

- Not recommended for new designs. For alternatives, see the Si533x family of products.
- Selectable output frequencies ranging from 19.44 to 1050 MHz
- Low jitter clock outputs w/jitter generation as low as 0.6 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (150 kHz to 1.3 MHz)
- Four clock inputs w/manual or automatically controlled switching
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOS alarm outputs
- Pin-programmable settings
- On-chip voltage regulator for 1.8 ±5%, 2.5 V ±10%, or 3.3 V ±10% operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS compliant

Ordering Information:
See page 21.

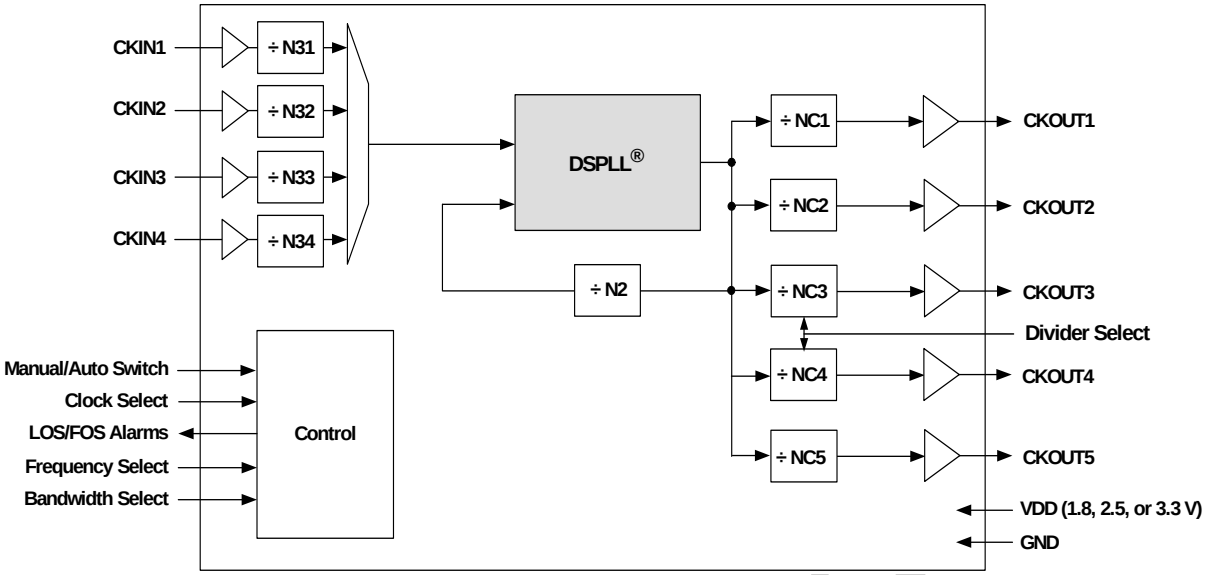
Applications

- SONET/SDH OC-48/STM-16 and STM-64/OC-192 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 line cards
- Test and measurement

Description

The Si5365 is a low-jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel, in which the application requires clock multiplication without jitter attenuation. The Si5365 accepts four clock inputs ranging from 19.44 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel frequencies. The Si5365 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5365 is ideal for providing clock multiplication in high performance timing applications.

Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1]	I_{DD}	LVPECL Format 622.08 MHz Out All CKOUTs Enabled	—	394	435	mA
		LVPECL Format 622.08 MHz Out 1 CKOUT Enabled	—	253	294	mA
		CMOS Format 19.44 MHz Out All CKOUTs Enabled	—	278	321	mA
		CMOS Format 19.44 MHz Out 1 CKOUT Enabled	—	229	261	mA
		Disable Mode	—	165	—	mA
CKINn Input Pins[2]						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ± 5%	0.9	—	1.4	V
		2.5 V ± 10%	1	—	1.7	V
		3.3 V ± 10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Single-Ended Input Voltage Swing (See Absolute Specs)	V_{ISE}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Differential Input Voltage Swing (See Absolute Specs)	V_{ID}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		fCKIN > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 1. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clocks (CKOUTn)[3]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} –1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single Ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD}-0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVPECL, LVDS	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V
Output Drive Current (CMOS driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally)	CKO_{IO}	V_{DD} = 1.8 V	—	7.5	—	mA
		V_{DD} = 3.3 V	—	32	—	mA

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 1. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V
3-Level Input Pins[4]						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}	See Note 4	–20	—	—	µA
Input Mid Current	I_{IMM}	See Note 4	–2	—	+2	µA
Input High Current	I_{IHH}	See Note 4	—	—	20	µA

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

Table 1. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	IO = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
Output Voltage Low		IO = 2 mA V_{DD} = 2.97 V	—	—	0.4	V
Output Voltage High	V_{OH}	IO = –2 mA V_{DD} = 1.71 V	V_{DD} – 0.4	—	—	V
Output Voltage High		IO = –2 mA V_{DD} = 2.97 V	V_{DD} – 0.4	—	—	V
Disabled Leakage Current	I_{OZ}	RSTb = 0	–100	—	100	µA

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.

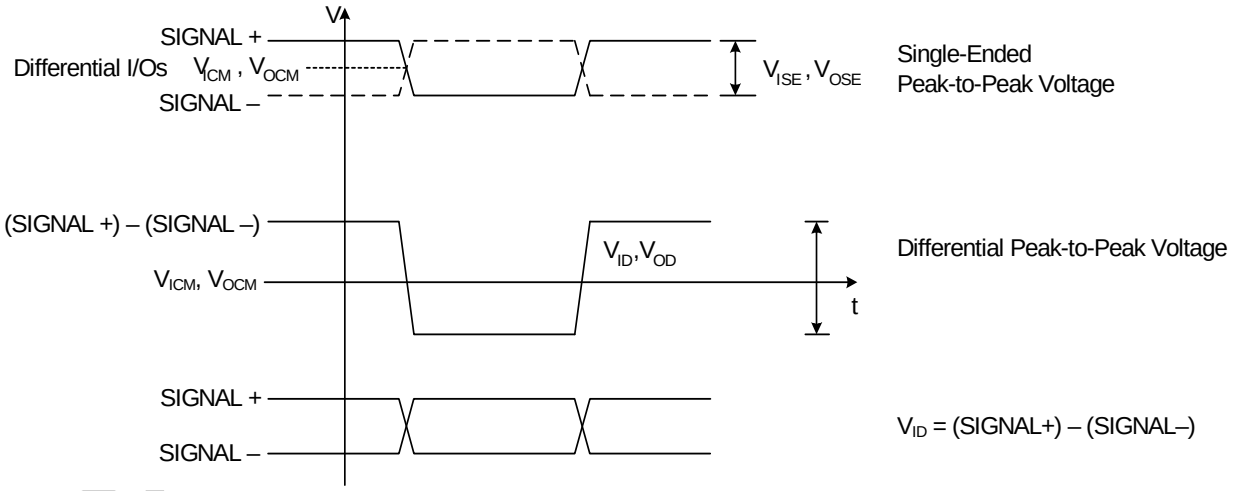


Figure 1. Differential Voltage Characteristics

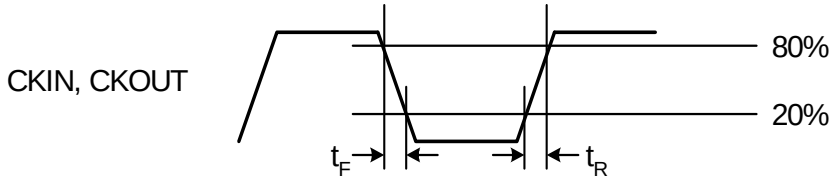


Figure 2. Rise/Fall Time Characteristics

Table 2. AC Specifications

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CKINn Input Pins						
Input Frequency	CKN_F		19.44	—	707.35	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins (See ordering section for speed grade vs frequency limits)						
Output Frequency (Output not configured for CMOS or Disabled)	CKO_F		19.44	—	1050	MHz
Maximum Output Frequency in CMOS Format	CKO_F		—	—	212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO_{TRF}	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 1.71 C_{LOAD} = 5 pF	—	—	8	ns
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 2.97 C_{LOAD} = 5 pF	—	—	2	ns
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO_{DC}	100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS)	—	—	+/-40	ps

Table 2. AC Specifications (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMN}		1			µs
Input Capacitance	C_{in}		—	—	3	pF
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20pf See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKINn ↑ to LOS↑	—	—	750	µs
Device Skew						
Output Clock Skew	t_{SKEW}	↑ of CKOUTn to ↑ of CKOUT_m, C	—	—	100	ps
Phase Change due to Temperature Variation	t_{TEMP}	Max phase changes from –40 to +85 °C	—	300	500	ps
PLL Performance **(fin=fout = 622.08 MHz; BW=120 Hz; LVPECL)**						
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise fout = 622.08 MHz	CKO_{PN}	1 kHz Offset	—	–90	—	dBc/Hz
		10 kHz Offset	—	–113	—	dBc/Hz
		100 kHz Offset	—	–118	—	dBc/Hz
		1 MHz Offset	—	–132	—	dBc/Hz
Spurious Noise	SP_{SPUR}	Max spur @ n x f3 (n ≥ 1, n x f3 < 100 MHz)	—	–93	–70	dBc

Table 3. Jitter Generation

Parameter	Symbol	Test Condition*		Min	Typ	Max	Unit
		Measurement Filter	DSPLL BW[2]				
Jitter Gen OC-192	JGEN	4–80 MHz	120 Hz	—	.23	—	ps_{rms}
		0.05–80 MHz	120 Hz	—	.47	—	ps rms
Jitter Gen OC-48	JGEN	0.12–20 MHz	120 Hz	—	.48	—	ps rms

***Note:** Test conditions:

1. fIN = fOUT = 622.08 MHz
2. Clock input: LVPECL
3. Clock output: LVPECL
4. PLL bandwidth: 877 kHz
5. V_{DD} = 3.3 V
6. T_A = 85 °C

Table 4. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	40	C°/W

Table 5. Absolute Maximum Limits

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.8	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
CKINn Voltage Level Limits	CKN_{VIN}	0 to V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}	0 to 1.2	V
Operating Junction Temperature	T_{JCT}	–55 to 150	C
Storage Temperature Range	T_{STG}	–55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–		2	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–		150	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–		700	V
ESD MM Tolerance; CKIN+/CKIN–		100	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

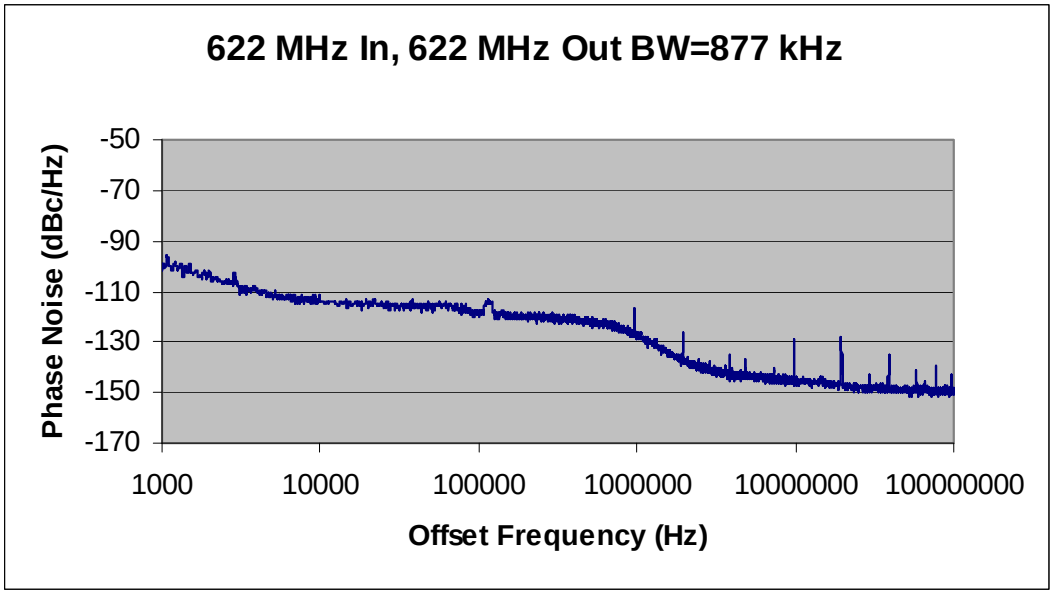
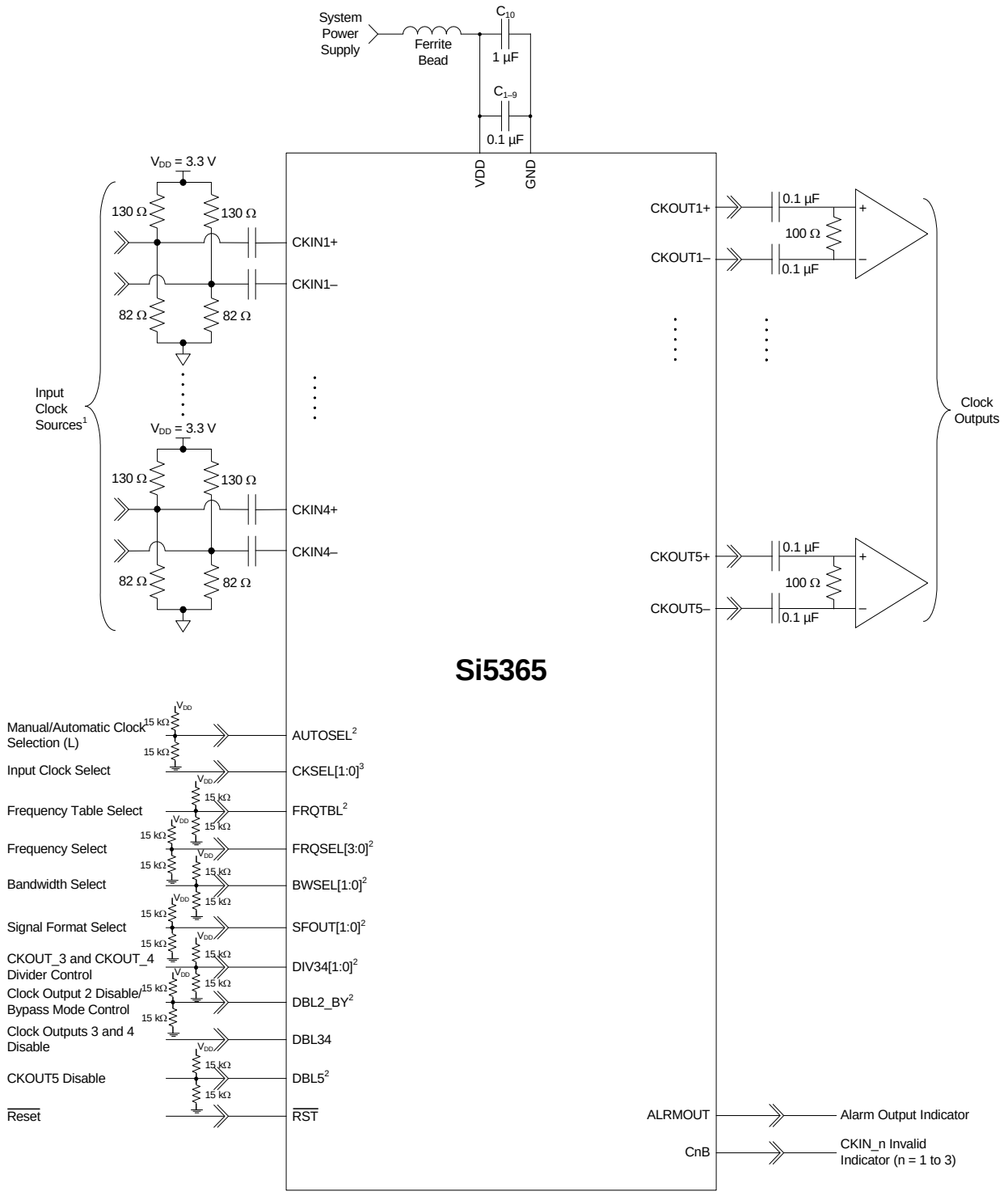


Figure 3. Typical Phase Noise Plot

Jitter Bandwidth	RMS Jitter (fs)
OC-48, 12 kHz to 20 MHz	374
OC-192, 20 kHz to 80 MHz	388
OC-192, 4 MHz to 80 MHz	181
OC-192, 50 kHz to 80 MHz	377
Broadband, 800 Hz to 80 MHz	420

2. Typical Application Schematic



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (V_{DD}/2), and H (V_{DD}).
3. Assumes manual input clock selection.

Figure 4. Si5365 Typical Application Circuit

3. Functional Description

The Si5365 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, SDH STM-16/STM-64, Ethernet, and Fibre Channel, in which the application requires clock multiplication without jitter attenuation. The Si5365 accepts four clock inputs ranging from 19.44 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. By default the four clock inputs are at the same frequency and the five clock outputs are at the same frequency. Two of the output clocks can be divided down further to generate an integer sub-multiple frequency. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel frequencies. In addition to providing clock multiplication in SONET and datacom applications, the Si5365 supports SONET-to-datacom frequency translations. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to look up valid Si5365 frequency translations. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5365 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5365 PLL loop bandwidth is digitally programmable via the BWSEL[1:0] pins and supports a range from 150 kHz to 1.3 MHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5365 monitors all input clocks for loss-of-signal and provides a LOS alarm when it detects a missing clock.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5365 has five differential clock outputs. The signal format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

3.1. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5365. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

4. Pin Descriptions: Si5365

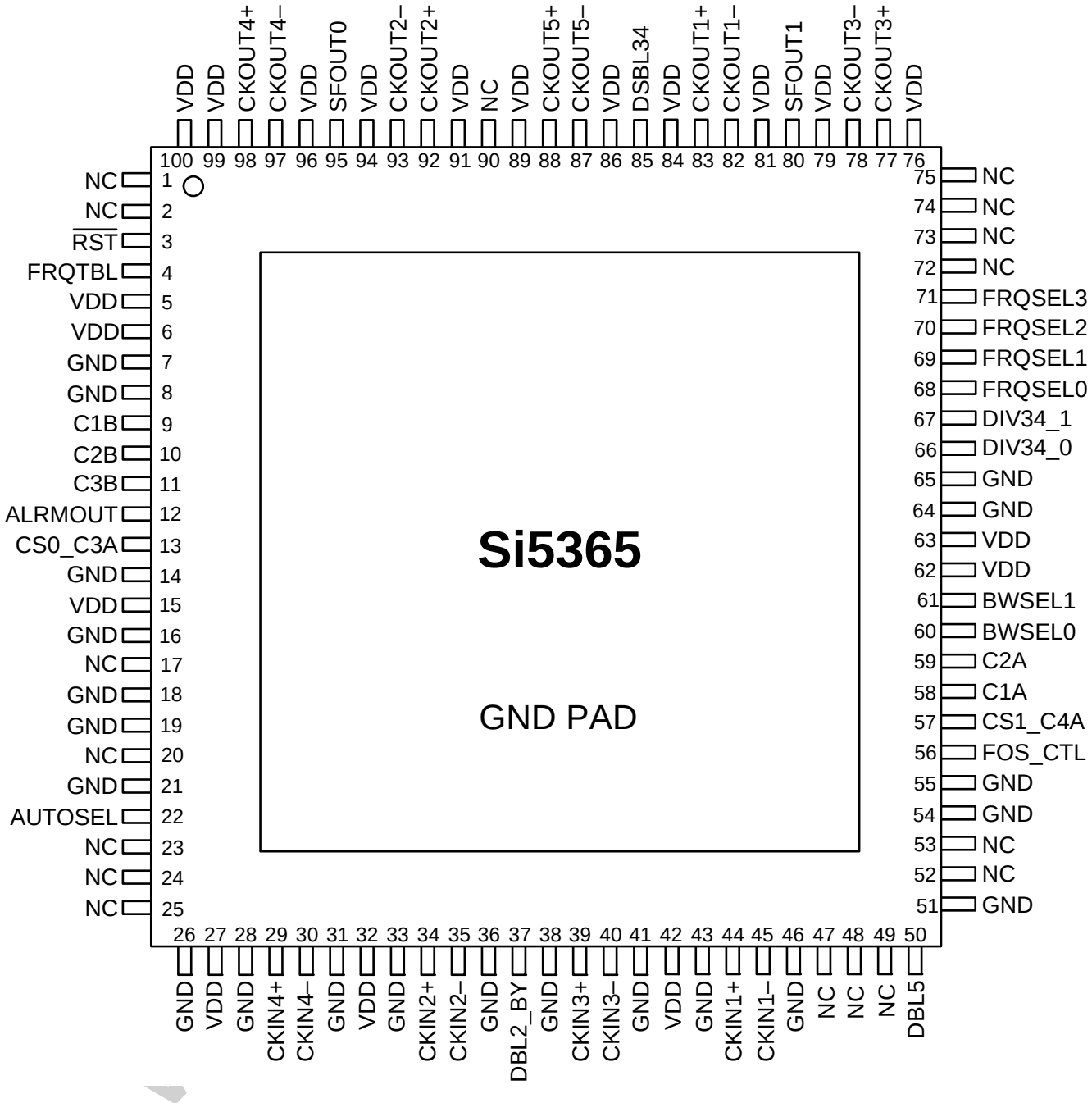


Table 6. Si5365 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1, 2, 17, 20, 23, 24, 25, 47, 48, 49, 52, 53, 72, 73, 74, 75, 90	NC			**No Connect.** These pins must be left unconnected for normal operation.
3	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. After rising edge of RST signal, the device will perform an internal self-calibration. This pin has a weak pullup.
4	FRQTBL	I	3-Level	**Frequency Table Select.** This pin selects SONET/SDH, datacom, or SONET/SDH to datacom frequency translation table. L = SONET/SDH. M = Datacom. H = SONET/SDH to Datacom. This pin has a weak pullup and weak pulldown and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
5, 6, 15, 27, 32, 42, 62, 63, 76, 79, 81, 84, 86, 89, 91, 94, 96, 99, 100	V_{DD}	V_{DD}	Supply	**V_{DD}.** The device operates from a 1.8 or 2.5 V supply. Bypass capacitors should be associated with the following V_{DD} pins: Pins — Bypass Cap 5, 6 — 0.1 µF 15 — 0.1 µF 27 — 0.1 µF 62, 63 — 0.1 µF 76, 79 — 1.0 µF 81, 84 — 0.1 µF 86, 89 — 0.1 µF 91, 94 — 0.1 µF 96, 99, 100 — 0.1 µF
7, 8, 14, 16, 18, 19, 21, 26, 28, 31, 33, 36, 38, 41, 43, 46, 51, 54, 55, 56, 64, 65	GND	GND	Supply	**Ground.** These pins must be connected to system ground. Minimize the ground path impedance for optimal performance.

Table 6. Si5365 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>9</td><td>C1B</td><td>O</td><td>LVCMOS</td><td>CKIN1 Invalid Indicator.
This pin is an active high alarm output associated with CKIN1. Once triggered, the alarm will remain high until CKIN1 is validated.
0 = No alarm on CKIN1.
1 = Alarm on CKIN1.</td></tr>
<tr><td>10</td><td>C2B</td><td>O</td><td>LVCMOS</td><td>CKIN2 Invalid Indicator.
This pin is an active high alarm output associated with CKIN2. Once triggered, the alarm will remain high until CKIN2 is validated.
0 = No alarm on CKIN2.
1 = Alarm on CKIN2.</td></tr>
<tr><td>11</td><td>C3B</td><td>O</td><td>LVCMOS</td><td>CKIN3 Invalid Indicator.
This pin is an active high alarm output associated with CKIN3.
0 = No alarm on CKIN3.
1 = Alarm on CKIN3.</td></tr>
<tr><td>12</td><td>ALRMOUT</td><td>O</td><td>LVCMOS</td><td>Alarm Output Indicator.
This pin is an active high alarm output associated with CKIN4 or the frame sync alignment alarm.
0 = ALRMOUT not active.
1 = ALRMOUT active.</td></tr>
<tr><td>13
57</td><td>CS0_C3A
CS1_C4A</td><td>I/O</td><td>LVCMOS</td><td>Input Clock Select/CKINn Active Clock Indicator.
Input: If manual clock selection mode is chosen (AUTOSEL = 1), the CS[1:0] pins function as the manual input clock selector control.
<table>
<tr><th>CS[1:0]</th><th>Active Input Clock</th></tr>
<tr><td>00</td><td>CKIN1</td></tr>
<tr><td>01</td><td>CKIN2</td></tr>
<tr><td>10</td><td>CKIN3</td></tr>
<tr><td>11</td><td>CKIN4</td></tr>
</table>
These inputs are internally deglitched to prevent inadvertent clock switching during changes in the CSn input state. If configured as input, these pins must not float.
Output: If automatic clock detection is chosen (AUTOSEL = M or H), these pins function as the CKINn active clock indicator output.
0 = CKINn is not the active input clock.
1 = CKINn is currently the active input clock to the PLL.
This pin has a weak pulldown.</td></tr>
<tr><td>22</td><td>AUTOSEL</td><td>I</td><td>3-Level</td><td>Manual/Automatic Clock Selection.
Three level input that selects the method of input clock selection to be used.
L = Manual.
M = Automatic non-revertive.
H = Automatic revertive.
This pin has a weak pullup and weak pulldown and defaults to M.
Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</td></tr>
<tr><td>29
30</td><td>CKIN4+
CKIN4–</td><td>I</td><td>MULTI</td><td>Clock Input 4.
Differential clock input. This input can also be driven with a single-ended signal.</td></tr>
</table>

Table 6. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
34 35	CKIN2+ CKIN2–	I	MULTI	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal.
37	DBL2_BY	I	3-Level	**CKOUT2 Disable/PLL Bypass Mode Control.** Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode. L = CKOUT2 Enabled. M = CKOUT2 Disabled. H = BYPASS Mode with CKOUT2 enabled. Bypass is not available with CMOS outputs. This pin has a weak pullup and weak pulldown and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
39 40	CKIN3+ CKIN3–	I	MULTI	**Clock Input 3.** Differential clock input. This input can also be driven with a single-ended signal.
44 45	CKIN1+ CKIN1–	I	MULTI	**Clock Input 1.** Differential clock input. This input can also be driven with a single-ended signal.
50	DBL5	I	3-Level	**CKOUT5 Disable.** This pin performs the following functions: L = Normal operation. Output path is active and signal format is determined by SFOUT inputs. M = CMOS signal format. Overrides SFOUT signal format to allow CKOUT5 to operate in CMOS format while the clock outputs operate in a differential output format. H = Powerdown. Entire CKOUT5 divider and output buffer path is powered down. CKOUT5 output will be in tristate mode during powerdown. This pin has a weak pullup and weak pulldown and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
56	FOS_CTL	I	3-Level	**Frequency Offset Control.** This pin enables or disables use of the CKIN2 FOS reference as an input to the clock selection state machine. L = FOS Disabled. M = Stratum 3/3E FOS Threshold. H = SONET Minimum Clock FOS Threshold. This pin has both weak pullups and weak pulldowns and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
58	C1A	O	LVCMOS	**CKIN1 Active Clock Indicator.** This pin serves as the CKIN1 active clock indicator. 0 = CKIN1 is not the active input clock. 1 = CKIN1 is currently the active input clock to the PLL.
59	C2A	O	LVCMOS	**CKIN2 Active Clock Indicator.** This pin serves as the CKIN2 active clock indicator. 0 = CKIN2 is not the active input clock. 1 = CKIN2 is currently the active input clock to the PLL.

Table 6. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
60 61	BWSEL0 BWSEL1	I	3-Level	**Bandwidth Select.** These pins are three level inputs that select the DSPLL closed loop bandwidth according to the Any-Frequency Precision Clock Family Reference Manual. These pins have both weak pullups and weak pulldowns and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
66 67	DIV34_0 DIV34_1	I	3-Level	**CKOUT3 and CKOUT4 Divider Control.** These pins control the division of CKOUT3 and CKOUT4 relative to the CKOUT2 output frequency. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. These pins have both weak pullups and weak pulldowns and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
68 69 70 71	FRQSEL0 FRQSEL1 FRQSEL2 FRQSEL3	I	3-Level	**Multiplier Select.** These pins are three level inputs that select the input clock and clock multiplication setting according to the Any-Frequency Precision Clock Family Reference Manual, depending on the FRQTBL setting. These pins have both weak pullups and weak pulldowns and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
77 78	CKOUT3+ CKOUT3–	O	MULTI	**Clock Output 3.** Differential output clock with a frequency specified by FRQSEL and FRQTBL settings. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.

Table 6. Si5365 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>80
95</td><td>SFOUT1
SFOUT0</td><td>I</td><td>3-Level</td><td>Signal Format Select.
Three level inputs that select the output signal format (common mode voltage and differential swing) for all of the clock outputs except CKOUT5 (see DBL5).
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>LVDS</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS—Low Swing</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Disable</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table>
Bypass mode is not available with CMOS outputs. When VDD = 3.3 V, for thermal reasons, there are restrictions on the number of LVPECL and CMOS outputs. See the Si53xx-RM reference manual for details.
These pins have both weak pullups and weak pulldowns and default to M.
Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</td></tr>
<tr><td>82
83</td><td>CKOUT1–
CKOUT1+</td><td>O</td><td>MULTI</td><td>Clock Output 1.
Differential output clock with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>85</td><td>DBL34</td><td>I</td><td>LVCMOS</td><td>Output 3 and 4 Disable.
Active high input. When active, entire CKOUT3 and CKOUT4 divider and output buffer path is powered down. CKOUT3 and CKOUT4 outputs will be in tristate mode during powerdown.
This pin has a weak pullup.</td></tr>
<tr><td>87
88</td><td>CKOUT5–
CKOUT5+</td><td>O</td><td>MULTI</td><td>Clock Output 5.
Fifth high-speed clock output with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>92
93</td><td>CKOUT2+
CKOUT2–</td><td>O</td><td>MULTI</td><td>Clock Output 2.
Differential output clock with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
</table>

Table 6. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
97 98	CKOUT4– CKOUT4+	O	MULTI	**Clock Output 4.** Differential output clock with a frequency specified by FRQSEL and FRQTBL settings. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
GND PAD	GND PAD	GND	Supply	**Ground Pad**. The ground pad must provide a low thermal and electrical impedance to a ground plane.

5. Ordering Guide

Ordering Part Number	Package	ROHS6, Pb-Free	Temperature Range
Si5365-C-GQ*	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C
***Note:** Not recommended for new designs. For alternatives, see the Si533x family.			

6. Package Outline: 100-Pin TQFP

Figure 5 illustrates the package details for the Si5365. Table 7 lists the values for the dimensions shown in the illustration.

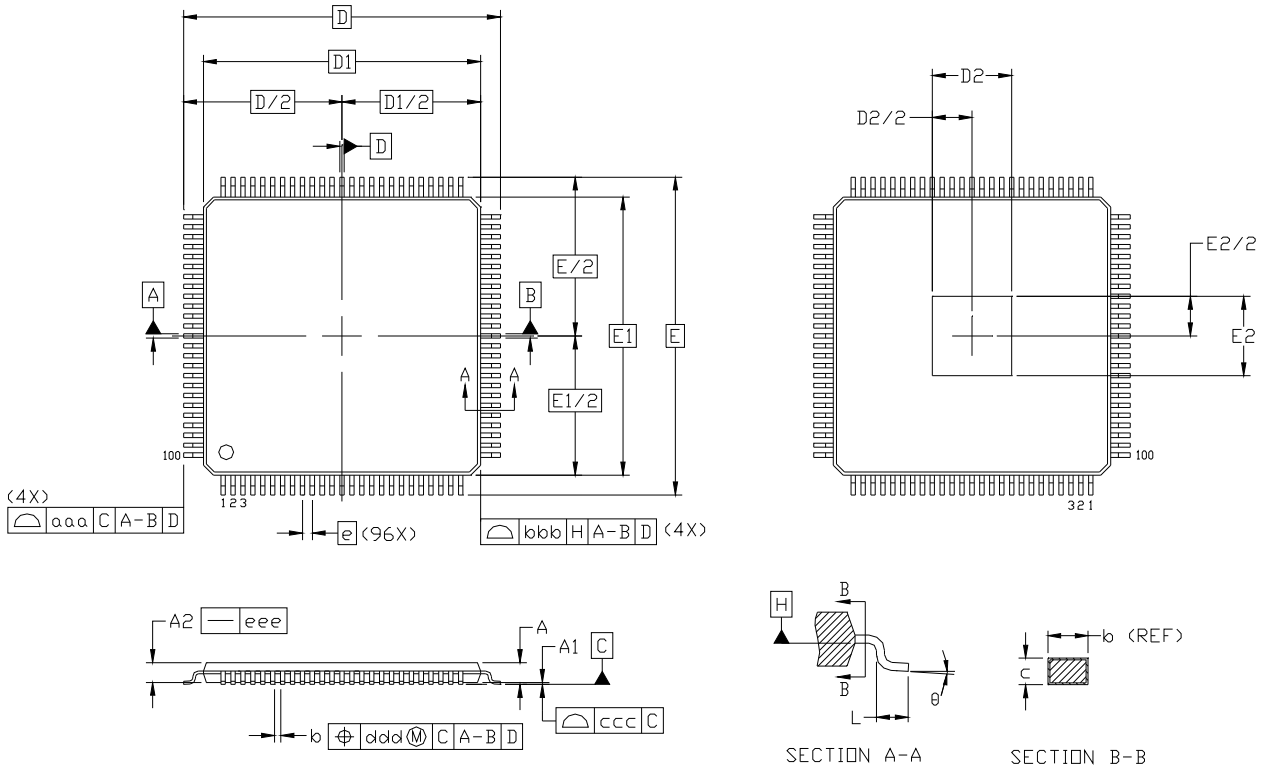


Figure 5. 100-Pin Thin Quad Flat Package (TQFP)

Table 7. 100-Pin Package Diagram Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
D2	3.85	4.00	4.15
e	0.50 BSC.		

Dimension	Min	Nom	Max
E	16.00 BSC.		
E1	14.00 BSC.		
E2	3.85	4.00	4.15
L	0.45	0.60	0.75
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08
Θ	0º	3.5º	7º

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant AED-HD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. PCB Land Pattern

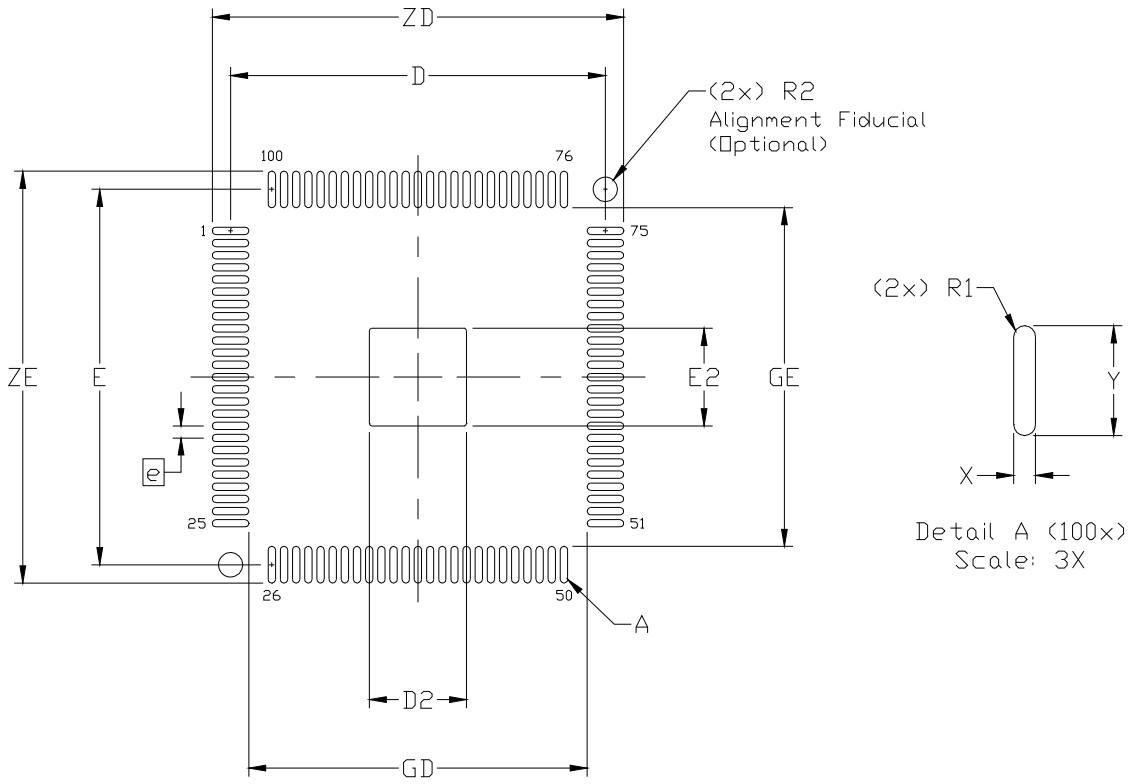


Figure 6. PCB Land Pattern Diagram

Table 8. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	15.40 REF.	
D	15.40 REF.	
E2	3.90	4.10
D2	3.90	4.10
GE	13.90	—
GD	13.90	—
X	—	0.30
Y	1.50 REF.	
ZE	—	16.90
ZD	—	16.90
R1	0.15 REF	
R2	—	1.00

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8. Top Marking

8.1. Si5365 Top Marking

8.2. Top Marking Explanation

Mark Method:	Laser	
Logo Size:	9.2 x 3.1 mm Center-Justified	
Font Size:	3.0 Point (1.07 mm) Right-Justified	
Line 1 Marking:	Device Part Number Si5365x-C-GQ	X = Speed Grade See "5. Ordering Guide" on page 21.
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly Supplier. Corresponds to the year and work-week of the mold date.
	R = Die Revision	
	TTTTT = Mfg Code	Manufacturing Code
Line 3 Marking:	Circle = 1.8 mm Diameter Center-Justified	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	

DOCUMENT CHANGE LIST

Revision 0.32 to Revision 0.33

- Condensed format.

Revision 0.33 to Revision 0.34

- Removed references to latency control, INC, and DEC pins.
- Updated Table 1, “Performance Specifications,” on page 2.
- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 3.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Updated Figure 4, “Si5365 Typical Application Circuit”.
- Updated “4. Pin Descriptions: Si5365”.
- Updated "5. Ordering Guide" on page 21.
- Added “7. PCB Land Pattern”.

Revision 0.34 to Revision 0.4

- Changed 1.8 V operating range to ±5%.
- Updated Table 1 on page 2.
- Updated Table 2 on page 3.
- Added page 4.
- Updated "3. Functional Description" on page 13.
- Clarified "4. Pin Descriptions: Si5365" on page 14 including the addition of FOS_CTL (pin 56).

Revision 0.4 to Revision 0.5

- Changed “rate” to “frequency” throughout.
- Added Table of Contents.
- Reordered and expanded spec tables.
- Added 3.3 V operation.
- Added "8. Top Marking" on page 25.
- Added no bypass with CMOS outputs.
- Updated Table 2, “AC Specifications,” on page 8.
- Updated Table 3, “Jitter Generation,” on page 10.
- Updated "5. Ordering Guide" on page 21.

NOTES:

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