MAX20002/MAX20003

36V, 220kHz to 2.2MHz, 2A/3A Fully Integrated Step-Down Converters with 15μA Operating Current

General Description

The MAX20002/MAX20003 are small, synchronous buck converters with integrated high-side and low-side MOSFETs. Each device is designed to deliver up to 2A/3A with input voltages from 3.5V to 36V, while using only 15μA quiescent current at no load. Voltage quality can be monitored by observing the PGOOD signal. The devices can operate in dropout by running at 98% duty cycle, making them ideal for automotive applications.

The devices offer fixed output voltages of 5V/3.3V, along with the ability to program the output voltage between 1V to 10V. Frequency can be programmed using a resistor to ground on the FOSC pin from 220kHz to 2.2MHz. The devices offer a forced fixed-frequency mode and skip mode with ultra-low quiescent current of 15μA. They have a pin that can be programmed to turn on/off the spread spectrum, further helping systems designers with better EMC management.

The MAX20002/MAX20003 are available in a small 5mm x 5mm 20-pin TQFN package with exposed pad and use very few external components.

Applications

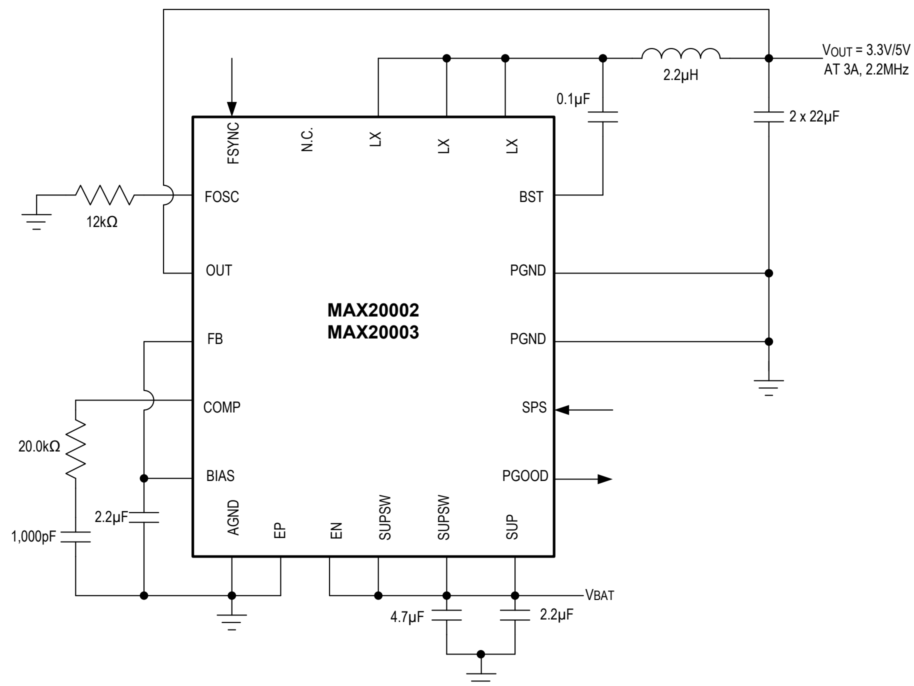
- Point-of-Load Applications in Automotive
- Distributed DC Power Systems
- Navigation and Radio Head Units

Benefits and Features

- Synchronous DC-DC Converter with Integrated FETs
  - MAX20002 = 2A
  - MAX20003 = 3A
  - 15μA Quiescent Current When in Standby Mode
- Small Solution Size Saves Space
  - 220kHz to 2.2MHz Adjustable Frequency
  - Programmable 1V to 10V Output for the Buck or Fixed 5V/3.3V Options Available
  - Fixed 8ms Internal Soft-Start
  - Fixed Output Voltage with ±2% Output Accuracy (5V/3.3V) or Externally Resistor Adjustable (1V to 10V) with ±1% FB Accuracy
- PGOOD Output and High-Voltage EN Input Simplify Power Sequencing
- Protection Features and Operating Range Ideal for Automotive Applications
  - Operating V_{IN} Range of 3.5V to 36V
  - 42V Load-Dump Protection
  - 99% Duty-Cycle Operation with Low Dropout
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified
  - Fast and Accurate Overvoltage Protection Enables Fast Recovery from Automotive Transients (MAX20002C/MAX20003C)

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit/Block Diagram



Absolute Maximum Ratings

SUP, SUPSW, LX, EN to PGND ....-0.3V to +42V
SUP to SUPSW ....-0.3V to +0.3V
BIAS to AGND ....-0.3V to +6V
SPS, FOSC, COMP to AGND ....-0.3V to (V_{BIAS} + 0.3V)
FSYNC, PGOOD, FB to AGND.............-0.3V to (V_{BIAS} + 0.3V)
OUT to PGND ....-0.3V to +12V
BST to LX ....-0.3V to +6V
AGND to PGND...-0.3V to +0.3V
Output Short-Circuit Duration ....Continuous
Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 33.3mW/°C above +70°C) ..2666.7mW
Operating Temperature Range........................ -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....30°C/W
Junction-to-Case Thermal Resistance (θ_{JC})................2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 2.2μH, C_{IN} = 4.7μF, C_{OUT} = 44μF, C_{BIAS} = 2.2μF, C_{BST} = 0.1μF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP}, V_{SUPSW}		3.5		36	V
Load-Dump Event Supply Voltage	V_{SUP_LD}	t_{LD} < 1s			42	V
Supply Current	$I_{SUP\_STANDBY}$	Standby mode, no load, V_{OUT} = 3.3V, V_{FSYNC} = 0V		15	30	μA
Supply Current (5V)	$I_{SUP\_STANDBY}$	Standby mode, no load, V_{OUT} = 5V, V_{FSYNC} = 0V		20	35	μA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V		5	10	μA
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = V_{SUPSW} = 6V to 42V, I_{BIAS} = 0 to 10mA	4.7	5	5.4	V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} rising	2.9	3.15	3.4	V
BIAS Undervoltage-Lockout Hysteresis				400	500	mV
Thermal-Shutdown Threshold				175		°C
Thermal-Shutdown Threshold Hysteresis				15		°C
OUTPUT VOLTAGE						
PWM-Mode Output Voltage (Note 2)	V_{OUT_5V}	V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V, fixed-frequency mode	4.9	5	5.1	V
	$V_{OUT\_3.3V}$		3.23	3.3	3.37	
Skip-Mode Output Voltage (Note 3)	$V_{OUT\_SKIP\_5V}$	No load, V_{FB} = V_{BIAS}, skip mode	4.9	5	5.15	V
	$V_{OUT\_SKIP\_3.3V}$		3.23	3.3	3.4	

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, VEN = 14V, L1 = 2.2μH, C_{IN} = 4.7μF, C_{OUT} = 44μF, C_{BIAS} = 2.2μF, C_{BST} = 0.1μF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Load Regulation		V_{FB} = V_{BIAS}, 30mA < I_{LOAD} < 3A		0.5		%
Line Regulation		V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V		0.02		%/V
BST Input Current	I_{BST_ON}	High-side MOSFET on, V_{BST} - V_{LX} = 5V		1.5		mA
	I_{BST_OFF}	High-side MOSFET off, V_{BST} - V_{LX} = 5V		1.5		μA
LX Current Limit	I_{LX}	MAX20003: MAX20003CATPA/V+, MAX20003CATPB/V+,	3.75	5	6.25	A
		MAX20002, MAX20002C	2.5	3.33	4.16	
		MAX20003CATPC/V+, MAX20003CATPD/V+	5			
LX Rise Time		V_{OUT} = 5V, 3.3V		4		ns
Spread Spectrum		Spread spectrum enabled		FOSC ±3%		
High-Side Switch On-Resistance	R_{ON_H}	I_{LX} = 0.5A, V_{BIAS} = 5V		60	140	mΩ
High-Side Switch Leakage Current		High-side MOSFET off, V_{SUP} = 36V, V_{LX} = 0V, T_A = +25°C		1	5	μA
Low-Side Switch On-Resistance	R_{ON_L}	I_{LX} = 0.5A, V_{BIAS} = 5V		35	70	mΩ
Low-Side Switch Leakage Current		Low-side MOSFET off, V_{SUP} = 36V, V_{LX} = 36V, T_A = +25°C		1	5	μA
FB Input Current	I_{FB}	T_A = +25°C		20	100	nA
FB Regulation Voltage	V_{FB}	FB connected to an external resistive divider, 6V < V_{SUPSW} < 36V	0.99	1	1.01	V
		FB connected to an external resistive divider, 6V < V_{SUPSW} < 36V (MAX20002C, MAX20003C)	0.985	1	1.015	
FB Line Regulation	ΔV_{LINE}	6V < V_{SUPSW} < 36V		0.02		%/V
Transconductance (from FB to COMP)	g_M	V_{FB} = 1V, V_{BIAS} = 5V		700		μS
Minimum On-Time	t_{ON_MIN}				80	ns
Maximum Duty Cycle	DC_{MAX}			98	99	%
Oscillator Frequency		R_{FOSC} = 73.2kΩ		400		kHz
		R_{FOSC} = 12kΩ	2.0	2.2	2.4	MHz
SYNC, EN, AND SPS LOGIC THRESHOLDS						
External Input Clock Acquisition Time	t_{FSYNC}			1		Cycle
External Input Clock Frequency		R_{FOSC} = 12kΩ (Note 4)	1.8		2.6	MHz
External Input Clock High Threshold	V_{FSYNC_HI}	V_{FSYNC} rising	1.4			V

Electrical Characteristics (continued)

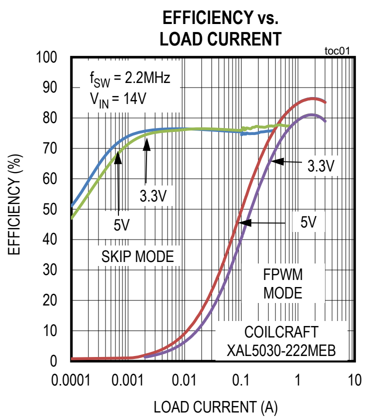
(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, L1 = 2.2µH, C_{IN} = 4.7µF, C_{OUT} = 44µF, C_{BIAS} = 2.2µF, C_{BST} = 0.1µF, R_{FOSC} = 12kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

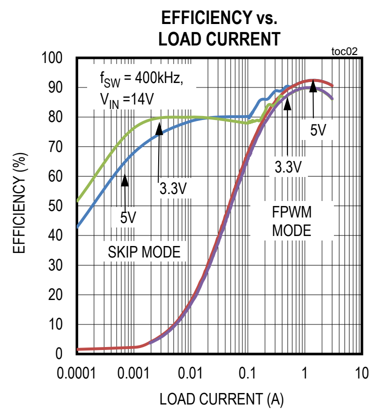
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Input Clock Low Threshold	V_{FSYNC_LO}	V_{FSYNC} falling			0.4	V
FSYNC Leakage Current		T_A = +25°C			1	µA
Soft-Start Time	t_{SS}		5.6	8	12	ms
Enable Input High Threshold	V_{EN_HI}		2.4			V
Enable Input Low Threshold	V_{EN_LO}				0.6	V
Enable Threshold Voltage Hysteresis	V_{EN_HYS}			0.2		V
Enable Input Current	I_{EN}	T_A = +25°C		0.1	1	µA
Spread-Spectrum Input High Threshold	V_{SPS_HI}		2.0			V
Spread-Spectrum Input Low Threshold	V_{SPS_LO}				0.4	V
Spread-Spectrum Input Current	I_{SPS}	T_A = +25°C		0.1	1	µA
POWER-GOOD AND OVERVOLTAGE-PROTECTION THRESOLDS						
PGOOD Switching Level	V_{RISING}	V_{FB} rising, V_{PGOOD} = high	93	95	97	%V_{FB}
	$V_{FALLING}$	V_{FB} falling, V_{PGOOD} = low	90	92.5	95	
PGOOD Debounce Time				25		µs
PGOOD Output Low Voltage		I_{SINK} = 5mA			0.4	V
PGOOD Leakage Current		V_{OUT} in regulation, T_A = +25°C			1	µA
Overvoltage-Protection Threshold		V_{OUT} rising (monitor FB pin)		107		%
		V_{OUT} falling (monitor FB pin)		104		

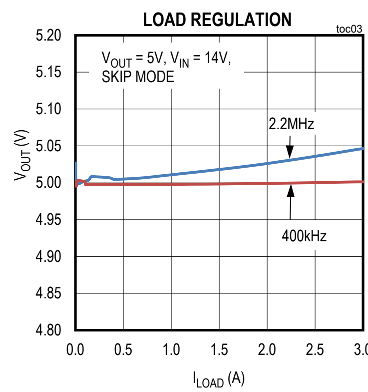
Note 2: Device not in dropout condition.
Note 3: Guaranteed by design; not production tested.
Note 4: Contact the factory for SYNC frequency outside the specified range.

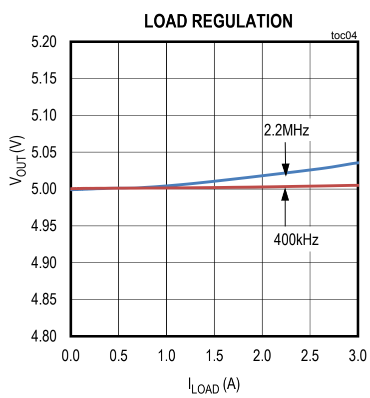
Typical Operating Characteristics

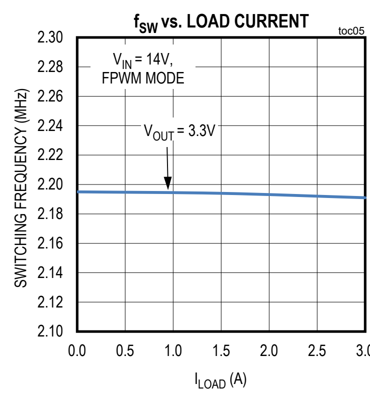
(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FSYNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

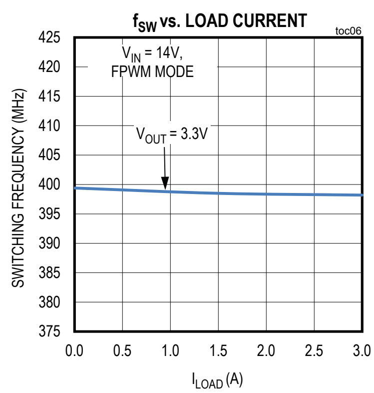


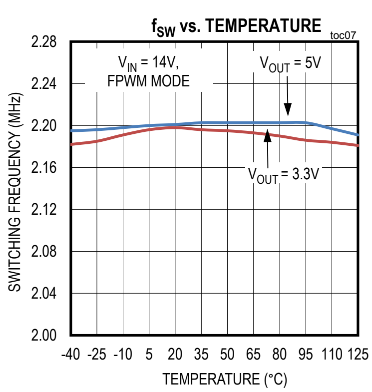


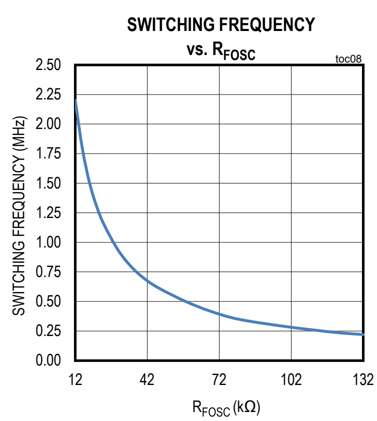


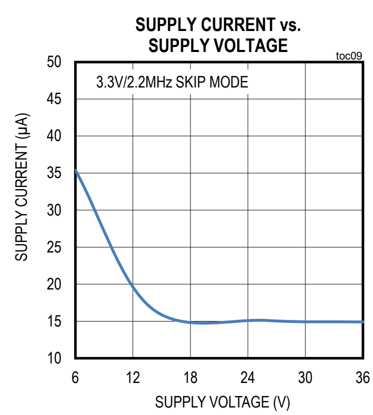






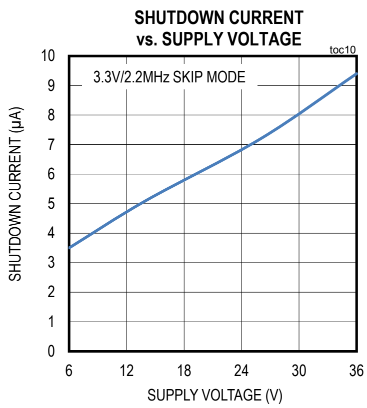


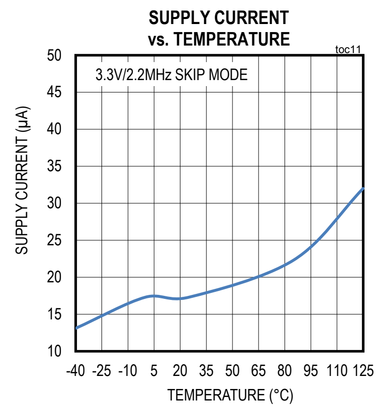


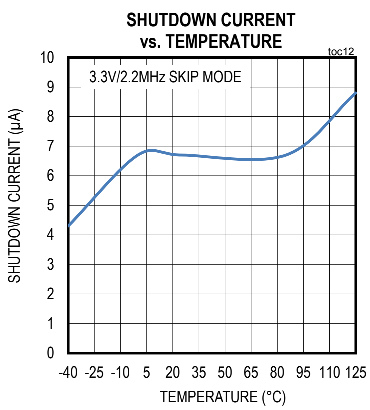


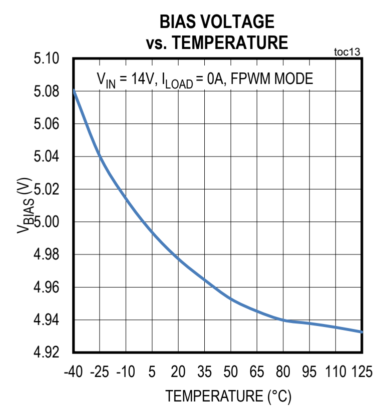
Typical Operating Characteristics (continued)

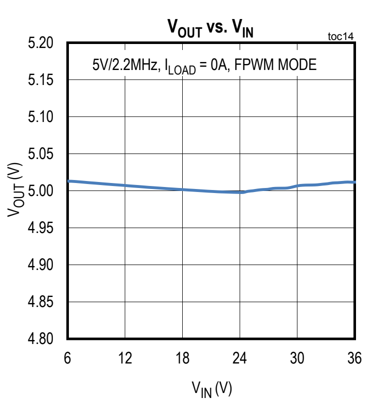
($V_{SUP} = V_{SUPSW}$ = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FSYNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

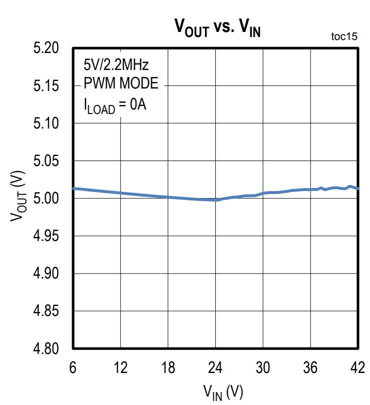








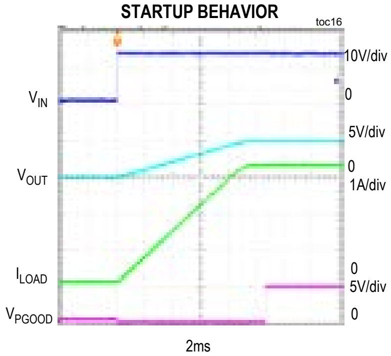




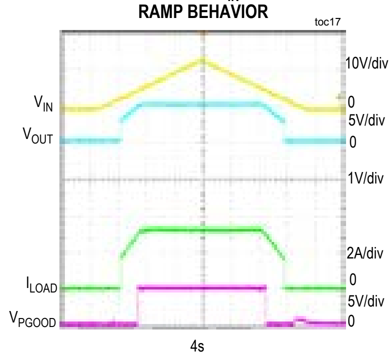
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FSYNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

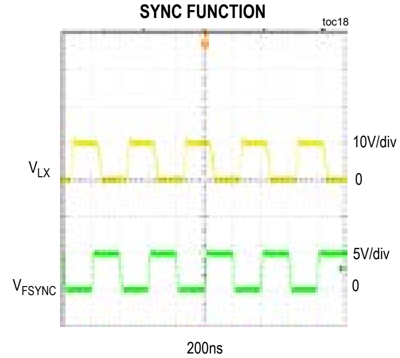
FULL-LOAD STARTUP BEHAVIOR



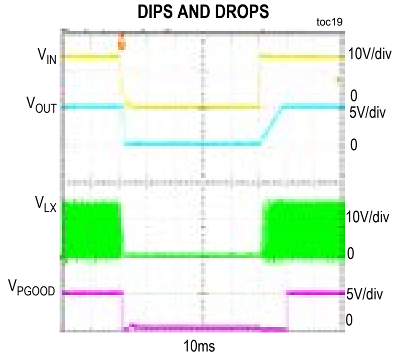
SLOW V_{IN} RAMP BEHAVIOR



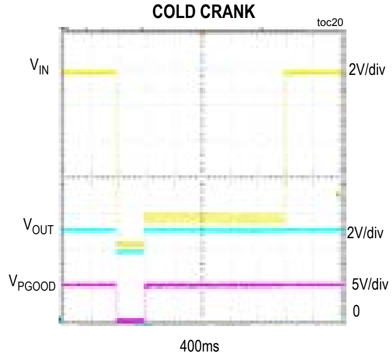
SYNC FUNCTION



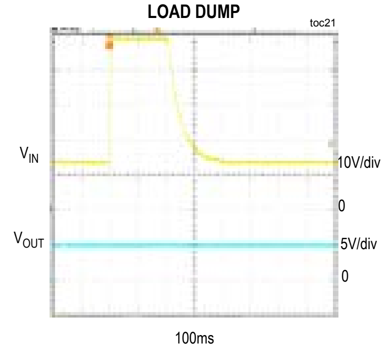
DIPS AND DROPS



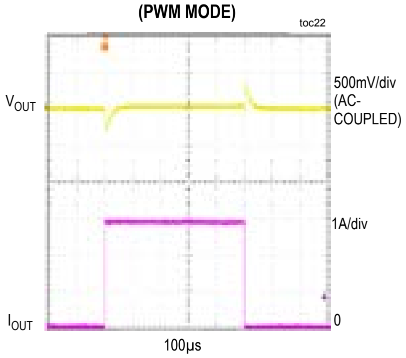
COLD CRANK



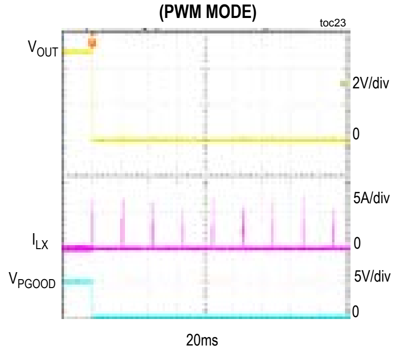
LOAD DUMP



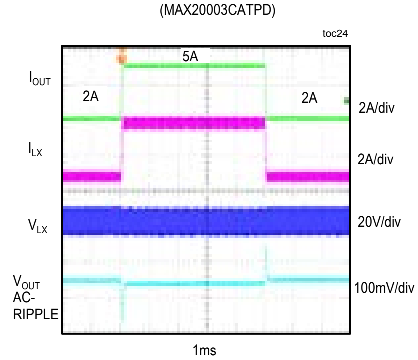
LOAD TRANSIENT (PWM MODE)



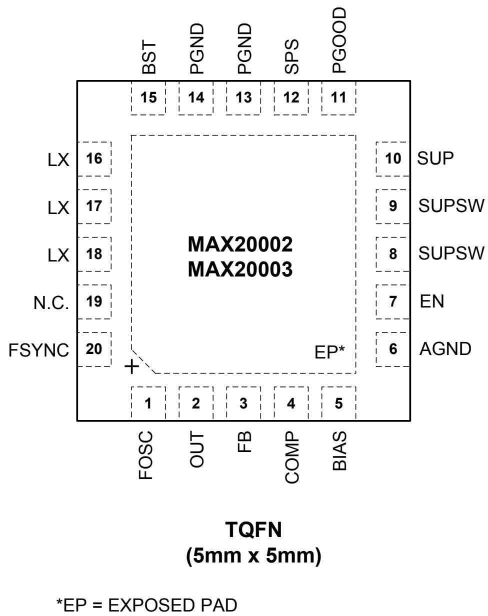
SHORT CIRCUIT (PWM MODE)



LOAD TRANSIENT RESPONSE (MAX20003CATPD)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	FOSC	Resistor-Programmable Switching-Frequency-Setting Control Input. Connect a resistor from FOSC to AGND to set the switching frequency.
2	OUT	Switching-Regulator Output. OUT also provides power to the internal circuitry when the output voltage of the converter is set between 3V to 5V during standby mode.
3	FB	Feedback Input. Connect an external resistive divider from OUT to FB and AGND to set the output voltage. Connect to BIAS to set the output voltage to 5V or 3.3V.
4	COMP	Error-Amplifier Output. Connect an RC network from COMP to AGND for stable operation. See the *Compensation Network* section for more details.
5	BIAS	Linear Regulator Output. BIAS powers up the internal circuitry. Bypass with a minimum of 2.2μF ceramic capacitor to ground.
6	AGND	Analog Ground
7	EN	SUP Voltage-Compatible Enable Input. Drive EN low to disable the devices. Drive EN high to enable the devices.
8, 9	SUPSW	Internal High-Side Switch Supply Input. SUPSW provides power to the internal switch. Bypass SUPSW to PGND with a 0.1μF and 4.7μF ceramic capacitors.
10	SUP	Voltage-Supply Input. SUP powers up the internal linear regulator. Bypass SUP to PGND with a 2.2μF ceramic capacitor.
11	PGOOD	Open-Drain, PGOOD Output. PGOOD asserts when V_{OUT} is above 95% regulation point. PGOOD goes low when V_{OUT} is below 92% regulation point.

Pin Description (continued)

PIN	NAME	FUNCTION
12	SPS	Spread-Spectrum Pin. Pull high for spread spectrum on and low for spread spectrum off.
13,14	PGND	Power Ground
15	BST	High-Side Driver Supply. Connect a 0.1μF capacitor between LX and BST for proper operation.
16–18	LX	Inductor Switching Node
19	N.C.	No Connection
20	FSYNC	Synchronization Input. The devices synchronize to an external signal applied to FSYNC. Connect FSYNC to AGND to enable skip mode operation. Connect to BIAS or to an external clock to enable fixed-frequency, forced-PWM mode operation. Do not leave the FSYNC pin unconnected.
—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP **must** be connected to PGND.

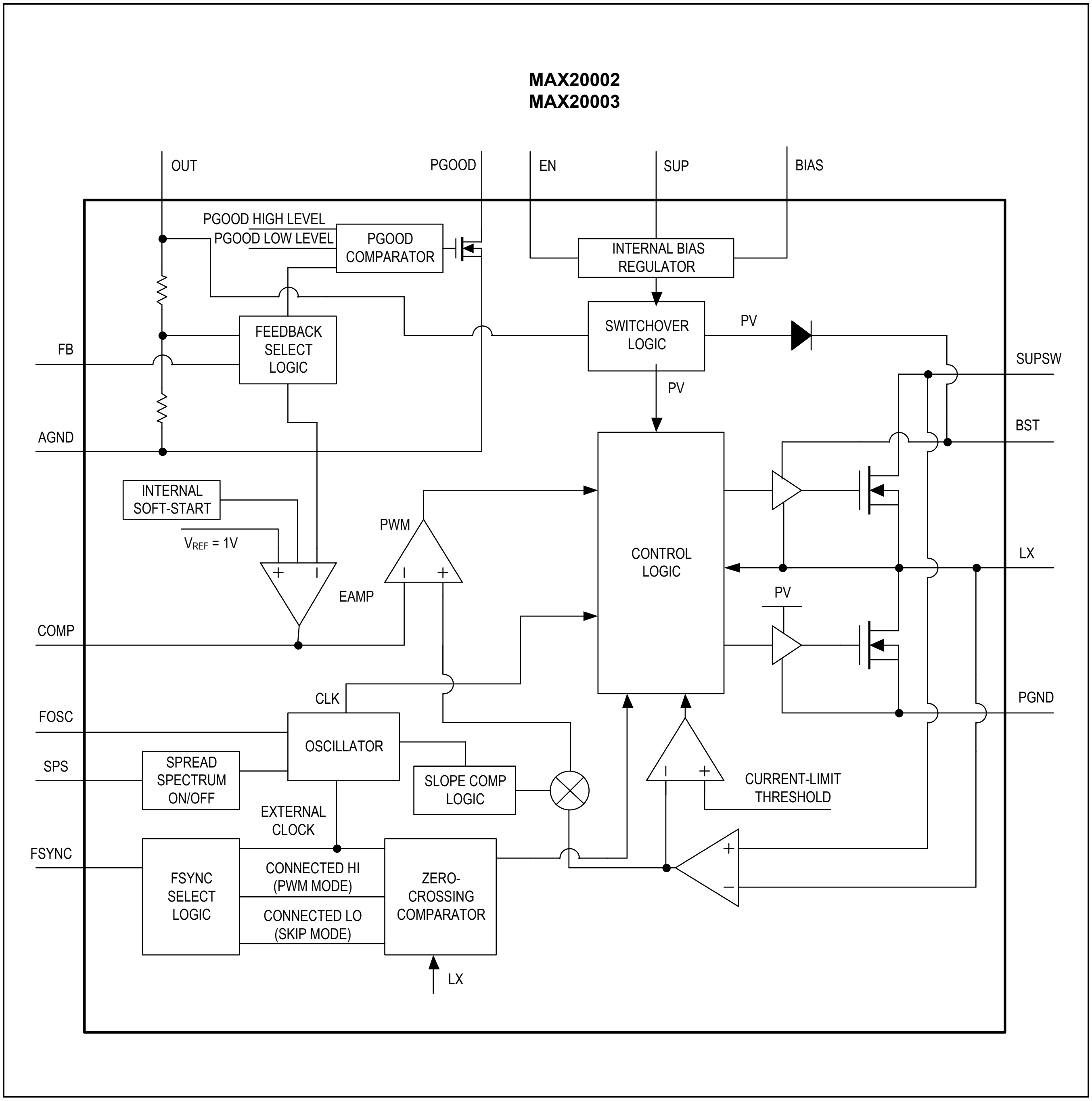


Figure 1. Internal Block Diagram

Detailed Description

The MAX20002/MAX20003 are 2A/3A current-mode step-down converters with integrated high-side and low-side MOSFETs. The low-side MOSFET enables fixed-frequency, forced-PWM operation in light-load applications. The devices operate with input voltages from 3.5V to 36V while using only 15μA quiescent current at no load. The switching frequency is resistor programmable from 220kHz to 2.2MHz and can be synchronized to an external clock. The devices' output voltage is available as 5V/3.3V fixed or adjustable from 1V to 10V. The wide input voltage range, along with its ability to operate at 99% duty cycle during undervoltage transients, makes the devices ideal for automotive applications.

In light-load applications, a logic input (FSYNC) allows the devices to operate either in skip mode for reduced current consumption, or fixed-frequency, forced-PWM mode to eliminate frequency variation and help minimize EMI. Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery. See Figure 1 for an internal block diagram.

Wide Input Voltage Range

The devices include two separate supply inputs (SUP and SUPSW) specified for a wide 3.5V to 36V input voltage range. V_{SUP} provides power to the device and V_{SUPSW} provides power to the internal switch. When the device is operating with a 3.5V input supply, conditions such as cold crank can cause the voltage at the SUP and SUPSW pins to drop below the programmed output voltage. Under such conditions, the devices operate in a high duty-cycle mode to facilitate minimum dropout from input to output.

Maximum Duty-Cycle Operation

The devices have a maximum duty cycle of 98% (typ). The IC monitors the off-time (time for which the low-side FET is on) in both PWM and skip modes every switching cycle. Once the off time of 100ns (typ) is detected continuously for 12μs, the low-side FET is forced on for 150ns (typ) every 12μs. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

The input voltage at which the devices enter dropout can be approximated as:

$$V_{SUP} = \frac{V_{OUT} + (I_{OUT} \times R_{ON\_H})}{0.98}$$

Note: The previous equation does not take into account the efficiency and switching frequency but is a good first-order approximation. Use the R_{ON_H} number from the maximum column in the *Electrical Characteristics* table.

Linear Regulator Output (BIAS)

The devices include a 5V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. Connect a 2.2μF ceramic capacitor from BIAS to AGND.

Power-Good Output (PGOOD)

The devices feature an open-drain power-good output (PGOOD). PGOOD asserts when V_{OUT} rises above 95% of its regulation voltage. PGOOD deasserts when V_{OUT} drops below 92.5% of its regulation voltage. Connect PGOOD to BIAS with a 10kΩ resistor.

Synchronization Input (FSYNC)

FSYNC is a logic-level input useful for operating-mode selection and frequency control. Connecting FSYNC to BIAS or to an external clock enables fixed-frequency, forced-PWM operation. Connecting FSYNC to AGND enables skip-mode operation.

The external clock frequency at FSYNC can be higher or lower than the internal clock by 20%. If the external clock frequency is greater than 120% of the internal clock, contact the factory applications team to verify the design. The devices synchronize to the external clock in two cycles. When the external clock signal at FSYNC is absent for more than two clock cycles, the devices use the internal clock.

System Enable (EN)

An enable control input (EN) activates the devices from their low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3.5V. The high-voltage compatibility allows EN to be connected to SUP, KEY/KL30, or the inhibit pin (INH) of a CAN transceiver.

EN turns on the internal regulator. Once V_{BIAS} is above the internal lockout threshold, V_{UVBIAS} = 3.15V (typ), the converter activates and the output voltage ramps up within 8ms.

A logic-low at EN shuts down the device. During shutdown, the internal linear regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 5μA (typ). Drive EN high to bring the devices out of shutdown.

Spread-Spectrum Option

The spread spectrum can be enabled on the device using a pin. When the SPS pin is pulled high the spread spectrum is enabled and the operating frequency is varied ±3% centered on FOSC. The modulation signal is a triangular wave with a period of 110µs at 2.2MHz. Therefore, FOSC ramps down 3% and back to 2.2MHz in 110µs and also ramps up 3% and back to 2.2MHz in 110µs. The cycle repeats.

For operations at FOSC values other than 2.2MHz, the modulation signal scales proportionally (e.g., at 400kHz, the 110µs modulation period increases to 110µs x 2.2MHz/0.4MHz = 550µs).

The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on the FSYNC pin and pass any modulation (including spread spectrum) present on the driving external clock.

Internal Oscillator (FOSC)

The switching frequency (f_{SW}) is set by a resistor (R_{FOSC}) connected from FOSC to AGND. For example, a 400kHz switching frequency is set with R_{FOSC} = 73.2kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds 175°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down converter, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Overvoltage Protection (OVP)

If the output voltage reaches the OVP threshold, the high-side switch is forced off and the low-side switch is forced on until the negative-current limit is reached. After negative-current limit is reached, both the high-side and low-side switches are turned off. The MAX20002C and MAX20003C feature an additional clamp and lower OVP threshold to limit the output-voltage overshoot for automotive conditions. Contact the Maxim Applications team to determine if the MAX20002C/MAX20003C are needed for your application.

Applications Information

Setting the Output Voltage

Connect FB to BIAS for a fixed +5V/3.3V output voltage. To set the output to other voltages between 1V and 10V, connect a resistive divider from output (OUT) to FB to AGND (Figure 2). Select R_{FB2} (FB to AGND resistor) less than or equal to 500kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} = 1V (see the *Electrical Characteristics* table).

Forced-PWM and Skip Modes

In PWM mode of operation, the devices switch at a constant frequency with variable on-time. In skip mode of operation, the converter's switching frequency is load dependent. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converters to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converters do not switch MOSFETs on and off as often as in the PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

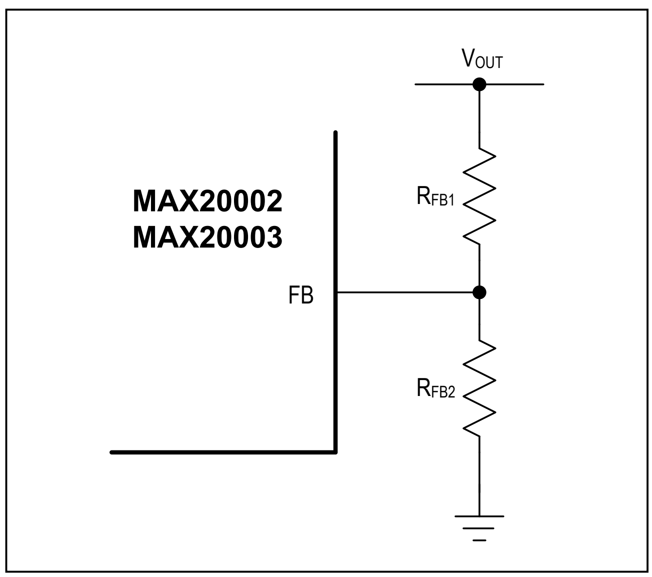


Figure 2. Adjustable Output-Voltage Setting

Inductor Selection

Three key inductor parameters must be specified for operation with the devices: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductor value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times I_{OUT} \times LIR}$$

where V_{SUP}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{FOSC} (see TOC 8 in the *Typical Operating Characteristics* section).

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} x (V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{V_{SUP}}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

$$D = \frac{V_{OUT}}{V_{SUPSW}}$$

where: I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output-ripple and load-transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage-fault protection. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple, so the size of the output capacitor depends on the maximum ESR required to meet the output-voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent voltage droop and voltage rise from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem. However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability.

Compensation Network

The devices use an internal transconductance error amplifier with its inverting input and its output available to the user for external frequency compensation. The output capacitor and compensation network determine the loop stability. The inductor and the output capacitor are chosen based on performance, size, and cost. Additionally, the compensation network optimizes the control-loop stability.

The converter uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. The devices use the voltage drop across the high-side MOSFET to sense inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. Only a simple single series resistor (R_C) and capacitor (C_C) are required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (see Figure 3). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output-capacitor loop, add another compensation capacitor (C_F) from COMP to ground to cancel this ESR zero.

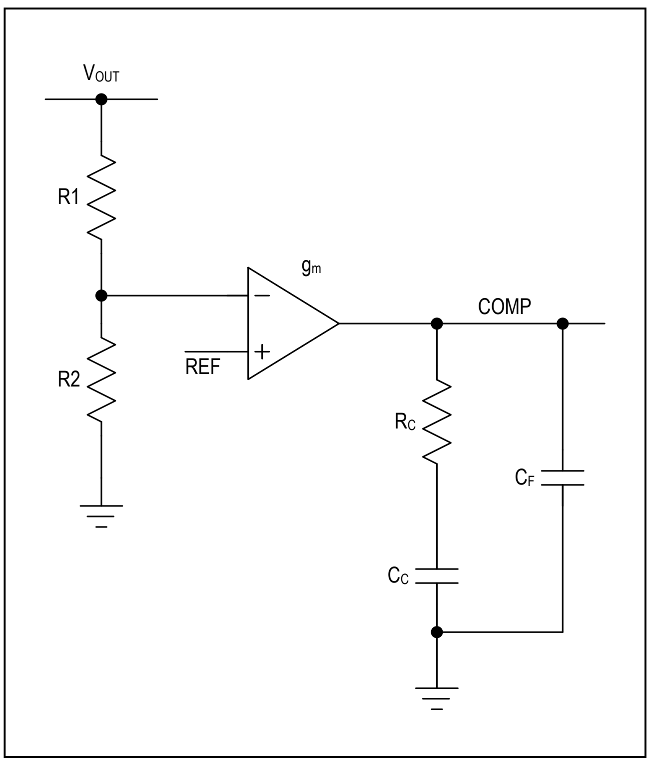


Figure 3. Compensation Network

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier. The power modulator has a DC gain set by $g_m \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The following equations help to approximate the value for the gain of the power modulator ($GAIN_{MOD(dc)}$), neglecting the effect of the ramp stabilization. Ramp stabilization is necessary when the duty cycle is above 50% and is internally done for the devices:

$$GAIN_{MOD(dc)} = g_{mc} \times R_{LOAD}$$

where $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$ in Ω and g_{mc} = 3S.

In a current-mode step-down converter, the output capacitor, its ESR, and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$, and $ESR = ESR_{(EACH)}/n$. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m\_EA} \times R_{OUT\_EA}$, where g_{m_EA} is the error amplifier transconductance, which is 700μS (typ), and R_{OUT_EA} is the output resistance of the error amplifier (50MΩ).

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance (R_{OUT_EA}). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{PEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C, where the loop gain equals 1 (0dB)). Thus:

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pdEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5 of the switching frequency and much higher than the power-modulator pole (f_{pMOD})

$$f_{pMOD} << f_C \leq \frac{f_{SW}}{5}$$

The total loop gain as the product of the modulator gain, the feedback voltage divider gain, and the error amplifier gain at f_C should be equal to 1. So:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(fC)} = 1$$

For the case where fzMOD is greater than f_C:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C a follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP to GND and set the compensation pole formed by R_C and C_F (f_{pEA}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same. For the case where f_{zMOD} is less than f_C:

The power-modulator gain at f_C is:

$$GAIN_{MOD(fC)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C} = 1$$

Solving for RC:

$$R_C = \frac{V_{OUT} \times f_C}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)} \times f_{zMOD}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD} ($f_{zEA} = f_{pMOD}$).

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 × f_C, add a second capacitor C_F from COMP to ground. Set $f_{pEA} = f_{zMOD}$ and calculate C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PC board layout:

1) Use a large contiguous copper plane under the device package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the devices must be soldered down to this copper plane for effective heat dissipation and getting the full power out of the devices. Use multiple vias or a single large via in this plane for heat dissipation
2) Isolate the power components and high current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible.
4) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
5) The analog signal lines should be routed away from the high-frequency planes. This ensures integrity of sensitive signals feeding back into the IC.
6) The ground connection for the analog and power section should be close to the IC. This keeps the ground current loops to a minimum. In cases where only one ground is used, adequate isolation between analog return signals and high-power signals must be maintained.

Ordering Information

PART	PIN-PACKAGE	V_{OUT} ADJUSTABLE (FB TIED TO RESISTOR-DIVIDER) (V)	V_{OUT} FIXED (FB TIED TO BIAS) (V)	MAXIMUM OPERATING CURRENT (A)	MINIMUM ILIM (A)	TIGHT OV THRESHOLD COMING OUT OF DROPOUT
MAX20002ATPA/V+	20 TQFN-EP*	1 to 10	5	2	2.5	No
MAX20002ATPB/V+	20 TQFN-EP*	1 to 10	3.3	2	2.5	No
MAX20002CATPA/V+	20 TQFN-EP*	1 to 10	5	2	2.5	Yes
MAX20002CATPB/V+	20 TQFN-EP*	1 to 10	3.3	2	2.5	Yes
MAX20003ATPA/V+	20 TQFN-EP*	1 to 10	5	3	3.75	No
MAX20003ATPB/V+	20 TQFN-EP*	1 to 10	3.3	3	3.75	No
MAX20003CATPA/V+	20 TQFN-EP*	1 to 10	5	3	3.75	Yes
MAX20003CATPB/V+	20 TQFN-EP*	1 to 10	3.3	3	3.75	Yes
MAX20003CATPC/V+	20 TQFN-EP*	1 to 10	5	3	5	Yes
MAX20003CATPD/V+	20 TQFN-EP*	1 to 10	3.3	3	5	Yes

Note: *All devices operate over the* -40°C to +125°C operating temperature range.
/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2055+4C	**21-0140**	**90-0009**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—
1	5/14	Added overvoltage protection threshold spec to *Electrical Characteristics* table	5
2	2/15	Updated the *Benefits and Features* section	1
3	11/15	Added new package variants to *Electrical Characteristics* and *Ordering Information* tables	4, 5, 17
4	3/16	Changed land pattern number in *Package Information* table from 90-0010 to 90-0009	17
5	4/16	Updated *Ordering Information*	18
6	6/16	Removed MAX20003CATPA/V+ and MAX20003CATPB/V+ from *Ordering Information*	18
7	6/16	Removed MAX20003CATPC/V+ and MAX20003CATPD/V+ from *Ordering Information*	18
8	9/16	Updated *Benefits and Features*; added new package variants in *Electrical Characteristics*, added TOC24 in *Typical Operating Characteristics*, updated FSYNC function in *Pin Description*; removed future product designations, added new package variants and Tight OV Threshold column in *Ordering Information*; added new *Overvoltage Protection (OVP) Thresholds* section	1, 4, 5, 8, 10, 13, 18

