

### Dual Channel Central Office ADSL2+ Line Driver

The ISL1536 is a very low power dual channel differential amplifier designed for central office line driving for DMT ADSL2+. This device features a high drive capability of 400mA while consuming only 4mA of supply current per amplifier from ±12V supplies. It integrates gain and bias resistors while maintaining high slew rate and low distortion.

### Ordering Information

| PART NUMBER<br>(Notes 1, 2, 3) | PART MARKING | TEMP. RANGE<br>(°C) | PACKAGE<br>(Pb-Free) | PKG. DWG. # |
|--------------------------------|--------------|---------------------|----------------------|-------------|
| ISL1536IRZ                     | 153 6IRZ     | -40 to +85          | 16 Ld QFN            | L16.4x4E    |
| ISL1536IRZ-T13*                | 153 6IRZ     | -40 to +85          | 16 Ld QFN            | L16.4x4E    |

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL1536](#). For more information on MSL, please see tech brief [TB363](#).

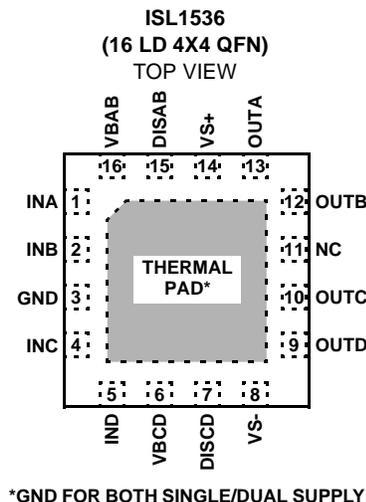
### Features

- Internal Fixed Gain  $A_V = 12.85$
- Integrated Feedback Resistors
- 43.4V<sub>P-P</sub> Differential Output Drive into 100Ω
- 41.6V<sub>P-P</sub> Minimum Differential Output Drive into 60Ω
- -59dBc Typical Driver Output Distortion Driving 50Ω at 2MHz
- Low Quiescent Current of 3mA per Amplifier
- Power-Down Disable Control
- Pb-Free (RoHS Compliant)

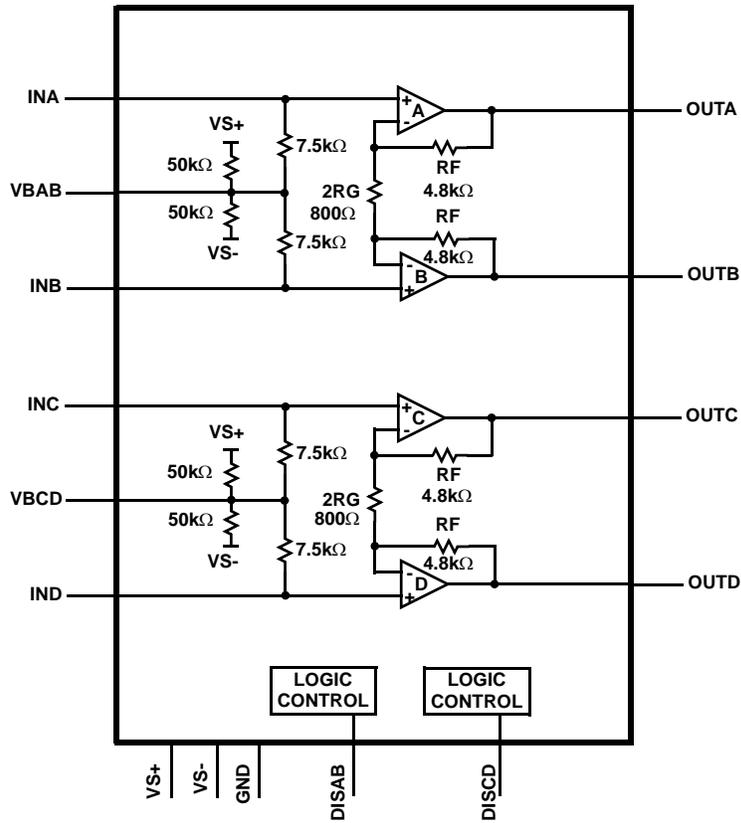
### Applications

- ADSL, ADSL2, ADSL2+ Line Drivers
- G.SHDSL, HDSL2 Line Drivers
- Video Distribution Amplifiers
- Video Twisted-pair Line Drivers

### Pinout



**Block Diagram**



**Pin Descriptions**

| 16 LD QFN | PIN NAME | FUNCTION   |
|-----------|----------|--|
| 1         | INA      | Amplifier A input                                |
| 2         | INB      | Amplifier B input                                |
| 3         | GND      | Ground connection                                |
| 4         | INC      | Amplifier C input                                |
| 5         | IND      | Amplifier D input                                |
| 6         | VBCD     | Voltage bias for amplifier C, D                  |
| 7         | DISCD    | Enable/disable amplifiers C, D (DSL Channel #2)  |
| 8         | VS-      | Negative supply                                  |
| 9         | OUTD     | Amplifier D output                               |
| 10        | OUTC     | Amplifier C output                               |
| 11        | NC       | No internal connection. Connect to GND on PCB.   |
| 12        | OUTB     | Amplifier B output                               |
| 13        | OUTA     | Amplifier A output                               |
| 14        | VS+      | Positive supply                                  |
| 15        | DISAB    | Enable/disable amplifiers A, B (DSL Channel #1). |
| 16        | VBAB     | Voltage bias for amplifier A, B                  |

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

|                                     |                      |
|-------------------------------------|----------------------|
| $V_{S+}$ to $V_{S-}$ Supply Voltage | 30V                  |
| $V_{S+}$ Voltage to Ground          | -0.3V to +30V        |
| $V_{S-}$ Voltage to Ground          | -30V to 0.3V         |
| Input DISAB, DISCD to Ground        | .7V                  |
| $V_{IN+}$ Voltage                   | $V_{S-}$ to $V_{S+}$ |
| Current into any Input              | 8mA                  |
| Continuous Output Current           | 75mA                 |
| <b>ESD Rating</b>                   |                      |
| Human Body Model                    | .4kV                 |
| Machine Model                       | .250V                |

**Thermal Information**

|                                      |   |
|--------------------------------------|---|
| Thermal Resistance (Typical, Note 4) | $\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )   |
| 16 Lead QFN                          | 40  |
| Ambient Operating Temperature Range  | -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$  |
| Storage Temperature Range            | -60 $^\circ\text{C}$ to +150 $^\circ\text{C}$   |
| Operating Junction Temperature       | +150 $^\circ\text{C}$   |
| Power Dissipation                    | See curves  |
| Pb-Free Reflow Profile               | see link below  |
|                                      | <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTE:**

4.  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications**  $V_S = \pm 12\text{V}$ ,  $R_L = 50\Omega$  to GND, DISAB = DISCD = 0,  $T_A = +25^\circ\text{C}$ , unless otherwise specified.

| PARAMETER                     | DESCRIPTION                      | CONDITIONS  | MIN (Note 5) | TYP         | MAX (Note 5) | UNIT                   |
|-------------------------------|----------------------------------|---|--------------|-------------|--------------|------------------------|
| <b>AC PERFORMANCE</b>         |                                  |   |              |             |              |                        |
| $A_V$                         | Gain                             |   | 12.6         | 12.85       | 13.1         | V/V                    |
| BW                            | -3dB Bandwidth                   |   |              | 50          |              | MHz                    |
| THD                           | Total Harmonic Distortion        | $f = 1\text{MHz}$ , $V_O = 10V_{O_{P-P}}$ - diff, $R_L = 50\Omega$ to GND   |              | -69         |              | dBc                    |
|                               |                                  | $f = 2.2\text{MHz}$ , $V_O = 10V_{O_{P-P}}$ - diff, $R_L = 50\Omega$ to GND |              | -59         |              | dBc                    |
| SR                            | Slew Rate, Single-Ended Signal   | $V_{OUT}$ from -4.5V to +4.5V   | 200          | 400         |              | V/ $\mu\text{s}$       |
| <b>DC PERFORMANCE</b>         |                                  |   |              |             |              |                        |
| $V_{OS-DM}$                   | Differential Mode Offset Voltage |   | -50          |             | +50          | mV                     |
| $V_{OS-CM}$                   | Common Mode Offset Voltage       |   | -125         |             | 125          | mV                     |
| <b>INPUT CHARACTERISTICS</b>  |                                  |   |              |             |              |                        |
| $I_{B+}$                      | Non-Inverting Input Bias Current |   | -5           |             | +5           | $\mu\text{A}$          |
| $e_N$                         | Input Noise Voltage              | $f = 10\text{kHz}$  |              | 8.0         |              | nV/ $\sqrt{\text{Hz}}$ |
| $i_{N+}$                      | +Input Noise Current             | $f = 10\text{kHz}$  |              | 1.0         |              | pA/ $\sqrt{\text{Hz}}$ |
| RIN                           | Input Resistance                 |   | 6            | 7.5         | 9            | k $\Omega$             |
| $V_{IH}$                      | Input High Voltage               | DIS inputs  | 2.2          |             |              | V                      |
| $V_{IL}$                      | Input Low Voltage                | DIS inputs  |              |             | 0.8          | V                      |
| $I_{IH}$                      | Input High Current for DIS       | DIS = 5V  | 20           | 58          | 100          | $\mu\text{A}$          |
| $I_{IL}$                      | Input Low Current for DIS        | DIS = 0V  | -25          | -7          | 0            | $\mu\text{A}$          |
| <b>OUTPUT CHARACTERISTICS</b> |                                  |   |              |             |              |                        |
| $V_{OUT-50}$                  | Loaded Output Swing Single-Ended | $R_L = 50\Omega$ to GND   | $\pm 10.4$   | $\pm 10.85$ |              | V                      |
| $V_{OUT-30}$                  | Loaded Output Swing Single-Ended | $R_L = 30\Omega$ to GND   | $\pm 9.8$    | $\pm 10.4$  |              | V                      |
| $V_{OUT-DIS}$                 | Disable Output Voltage           |   |              |             | $\pm 800$    | mV                     |
| $I_{OUT}$                     | Output Current                   | $R_L = 0\Omega$   |              | 600         |              | mA                     |

**Electrical Specifications**  $V_S = \pm 12V$ ,  $R_L = 50\Omega$  to GND, DISAB = DISCD = 0,  $T_A = +25^\circ C$ , unless otherwise specified. (Continued)

| PARAMETER                     | DESCRIPTION                           | CONDITIONS                  | MIN (Note 5) | TYP        | MAX (Note 5) | UNIT |
|-------------------------------|---------------------------------------|-----------------------------|--------------|------------|--------------|------|
| <b>SUPPLY CHARACTERISTICS</b> |                                       |                             |              |            |              |      |
| $V_{S(MAX)}$                  | Maximum Operating Supply Voltage      |                             |              | $\pm 13.2$ |              | V    |
| $V_{S(MIN)}$                  | Minimum Operating Supply Voltage      |                             |              | $\pm 7.5$  |              | V    |
| $I_{S^+}$ (Enable)            | Positive Supply Current per Amplifier | All outputs at 0V, DIS = 0V |              | 4.0        | 5            | mA   |
| $I_{S^-}$ (Enable)            | Negative Supply Current per Amplifier | All outputs at 0V, DIS = 0V | -4.85        | -3.9       |              | mA   |
| $I_{S^+}$ (Power Down)        | Positive Supply Current per Amplifier | All outputs at 0V, DIS = 5V |              | 0.3        | 0.75         | mA   |
| $I_{S^-}$ (Power Down)        | Negative Supply Current per Amplifier | All outputs at 0V, DIS = 5V | -0.75        | 0          |              | mA   |
| $I_{GND}$                     | GND Supply Current per Amplifier      | All outputs at 0V           |              | 0.3        |              | mA   |

NOTE:

- 5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

**Typical Performance Curves**

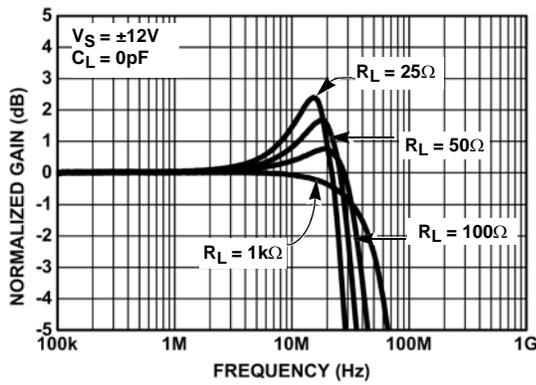


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE vs  $R_L$

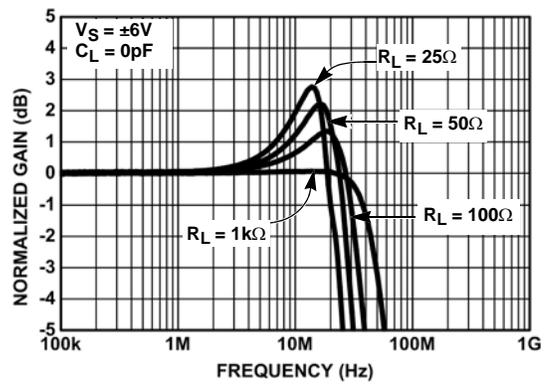


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE vs  $R_L$

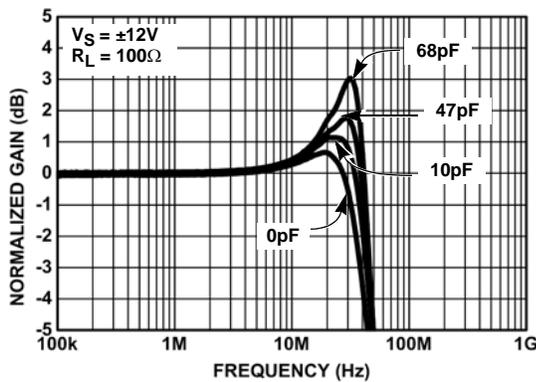


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE vs  $C_L$

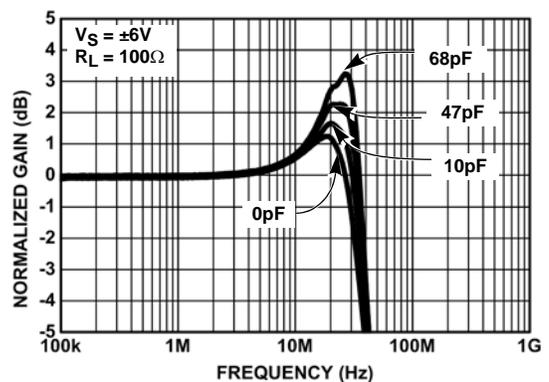


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE vs  $C_L$

Typical Performance Curves (Continued)

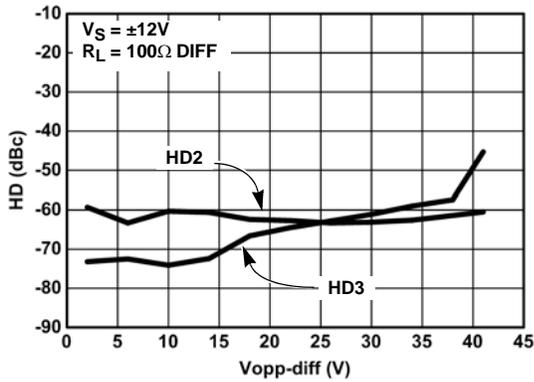


FIGURE 5. 200kHz 2ND AND 3RD HARMONICS vs DIFFERENTIAL OUTPUT VOLTAGE

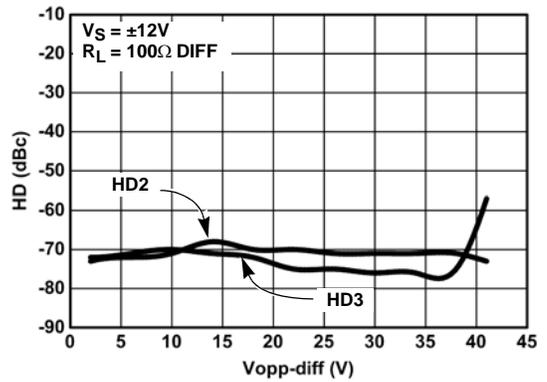


FIGURE 6. 1MHz 2ND AND 3RD HARMONICS vs DIFFERENTIAL OUTPUT VOLTAGE

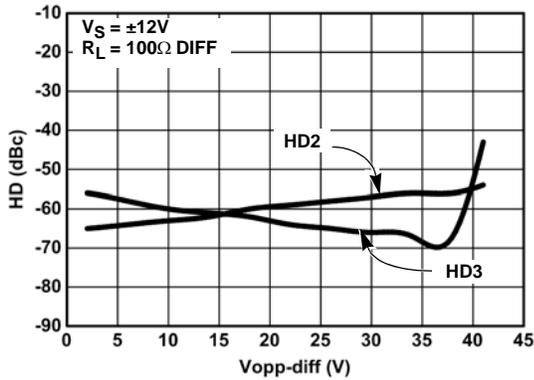


FIGURE 7. 2.2MHz 2ND AND 3RD HARMONICS vs DIFFERENTIAL OUTPUT VOLTAGE

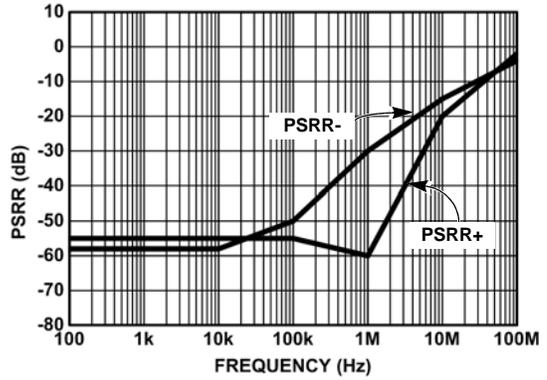


FIGURE 8. PSRR vs FREQUENCY

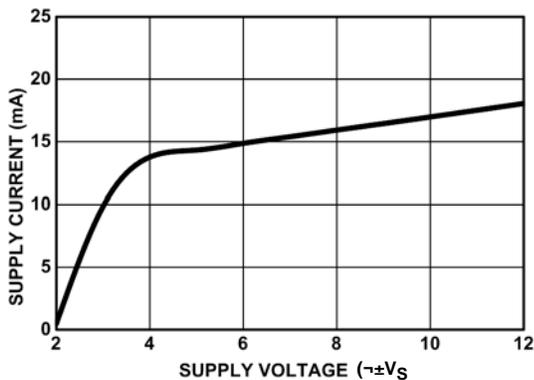


FIGURE 9. SUPPLY CURRENT vs SUPPLY VOLTAGE (ALL AMPLIFIERS ENABLED)

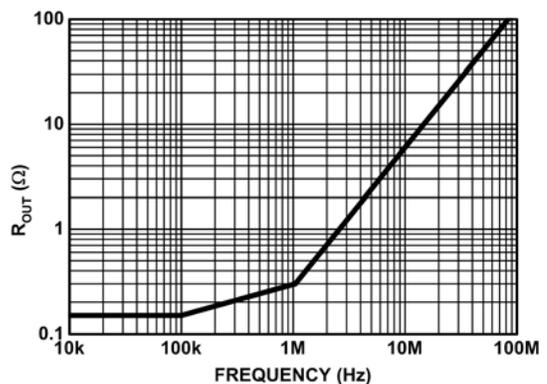


FIGURE 10. OUTPUT IMPEDANCE vs FREQUENCY

**Typical Performance Curves** (Continued)

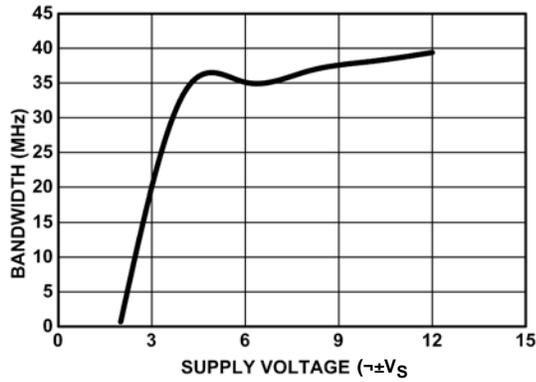


FIGURE 11. DIFFERENTIAL 3dB BANDWIDTH vs SUPPLY VOLTAGE

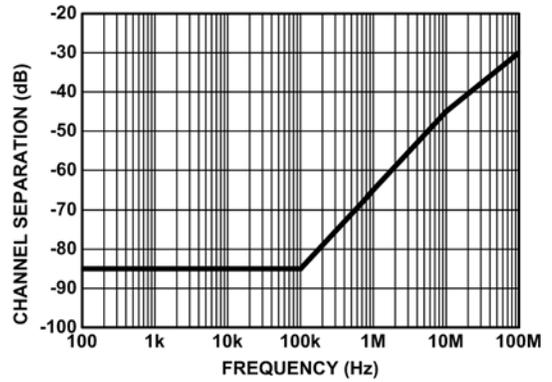


FIGURE 12. CHANNEL SEPARATION vs FREQUENCY

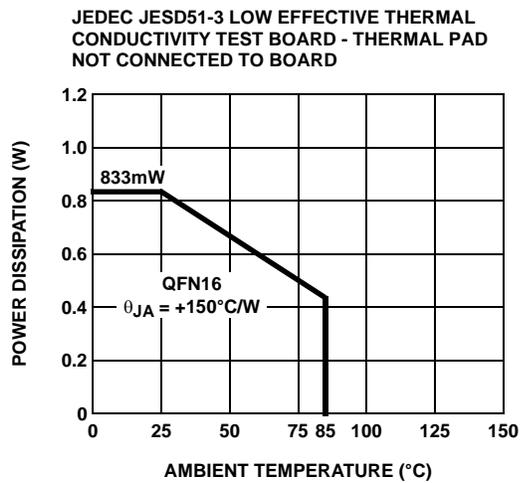


FIGURE 13. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

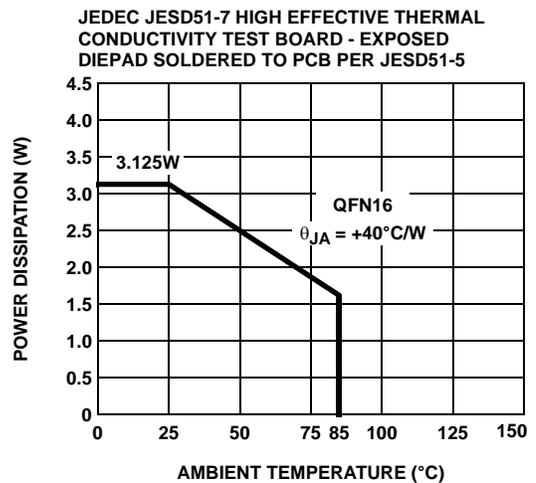


FIGURE 14. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## Applications Information

### Product Description

The ISL1536 consists of two sets of high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with ADSL2+ signals up to 2.2MHz. Each amplifier has identical positive gain connections resulting in optimum common-mode rejection. A typical interface circuit configuration is shown in Figure 15.

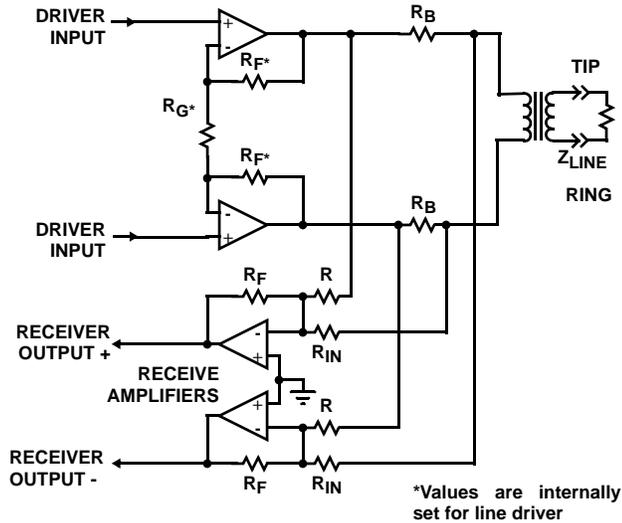


FIGURE 15. TYPICAL INTERFACE CIRCUIT CONFIGURATION

### Integrated Components

ISL1536 integrates bias and feedback resistors, minimizing the number of external components. The gain is fixed at +12.85V/V.

The VBAB and VBCD pins also integrate a pair of 7.5kΩ and 50kΩ resistors on each port to bias the line driver for single and dual supply usage. When powering the line driver with a single supply, VBAB and VBCD pins are floated. When using dual supplies, VBAB and VBCD pins are grounded.

Integration of these components in the line driver minimizes assembly cost and board space.

### Impedance Matching

$R_B$  in Figure 15 depends on the line impedance and transformer's turns ratio. Line impedance is characterized to be 100Ω across tip and ring. If a 1:N transformer is used,  $R_B$  can be calculated according to Equation 1:

$$\left( R_B = \frac{100}{N^2} \times 0.5 \right) \quad (\text{EQ. 1})$$

## Revision History

| DATE              | REVISION | CHANGE  |
|-------------------|----------|---|
| November 20, 2012 | FN6508.4 | Added Note 3 to "Ordering Information" on page 1.<br>Changed HBM from 3kV to 4kV in "Absolute Maximum Ratings" on page 3.<br>Changed MM from 300V to 250V in "Absolute Maximum Ratings" on page 3<br>Added Note 5 to "Electrical Specifications" table on page 4.   |
| March 8, 2010     | FN6508.3 | On page 4, changed the "Maximum Operating Supply Voltage" TYP from $\pm 12.6V$ to $\pm 13.2V$   |
| February 8, 2010  |          | On page 3 in the "Electrical Specifications" table, changed $V_{OUT-DIS}$ Max spec from $\pm 300mV$ to $\pm 800mV$  |
| May 29, 2009      |          | <p>Added Revision History beginning from rev 3.</p> <p>Changed the logic high level (VIH) on page 3 from Min 2.0V to Min 2.2V, which is consistent with the intended applications (AFE output logic high levels are typically at 3.3V with 2.4V minimum) while providing added margin to internal threshold variation.</p> <p>On page 1 in the first paragraph, changed: "This device features a high drive capability of 400mA while consuming only 3mA..." to "This device features a high drive capability of 400mA while consuming only 4mA..."</p> <p>Added Theta JA and applicable note to "Thermal Information" on page 3.</p> <p>Removed VS, Supply Voltage row in spec table. Added Maximum and Minimum Operating Supply Voltages (<math>V_{S(MAX)}</math> and <math>V_{S(MIN)}</math>) with typical specs of <math>\pm 12.6V</math> and <math>\pm 7.5V</math> to "SUPPLY CHARACTERISTICS" on page 4.</p> <p>Added "DISAB = DISCD = 0" to "Electrical Specifications" table common conditions.</p> |

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

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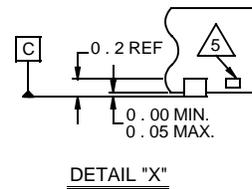
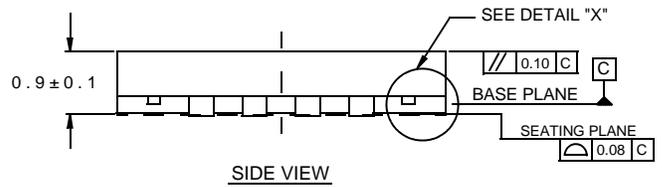
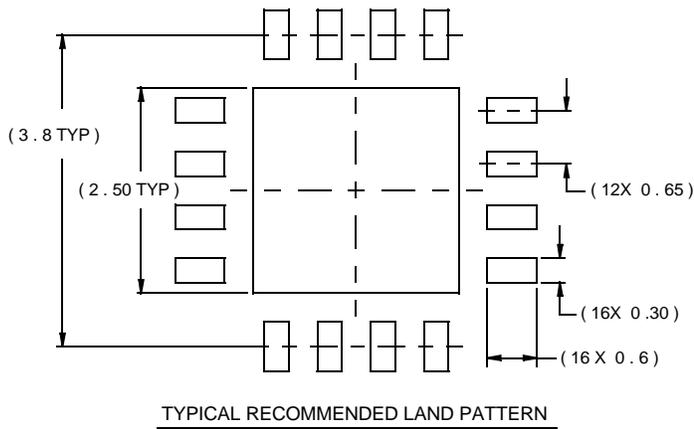
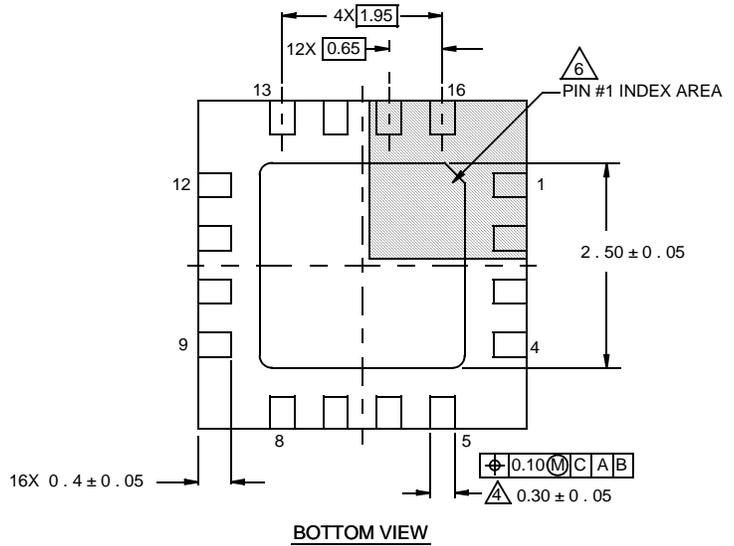
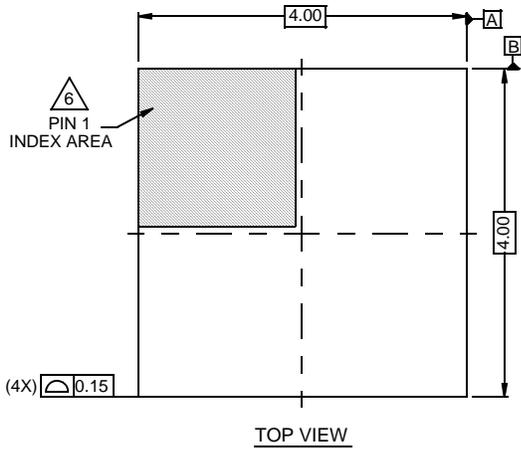
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# Package Outline Drawing

## L16.4x4E

### 16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 4/08



NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.