

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7USB31FK

Dual SPST USB Switch

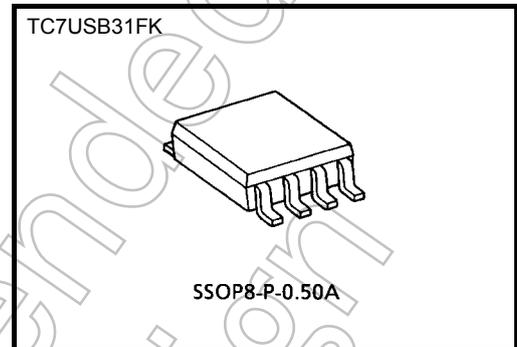
TC7USB31 is high-speed CMOS dual SPST USB Switch. The low ON-resistance and the low capacitance of the switch allow connections to USB application.

The TC7USB31 requires the output enable (\overline{OE}) input to be set high to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge.

Features

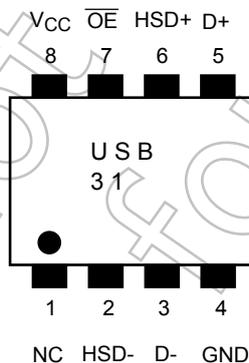
- Operating voltage: $V_{CC} = 2.3$ to 3.6 V
- ON-capacitance: $C_{I/O} = 4$ pF Switch ON (typ.) @ $V_{CC} = 3.3$ V
- ON-resistance: $R_{ON} = 4.5 \Omega$ (typ.) @ $V_{CC} = 3$ V, $V_{I/O} = 0$ V
- RON Flatness: $R_{ON(Flat)} = 1.2 \Omega$ (typ.) @ $V_{CC} = 3$ V
- Delta RON: $\Delta R_{ON} = 0.5 \Omega$ (typ.) @ $V_{CC} = 3$ V
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Power-down protection for inputs (\overline{OE} and I/O)
- Package : US8



Weight
SSOP8-P-0.50A : 0.01 g (typ)

Pin Assignment (top view)

FK (SSOP8-P-0.50A)

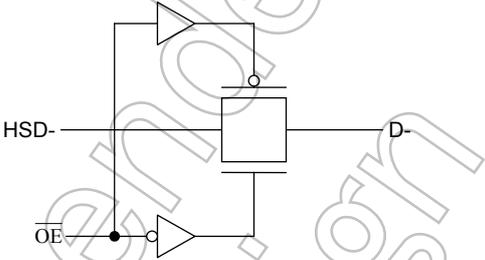
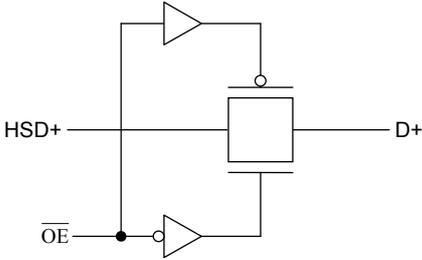


Start of commercial production
2009-09

Truth Table

Inputs		Function
\overline{OE}		
L		A port = B port
H		Disconnect

System Diagram



Not Recommended for New Design

Absolute Maximum Ratings (Note)

Characteristic		Symbol	Rating	Unit
Power supply range		V_{CC}	-0.5 to 4.6	V
Control pin input voltage (\overline{OE})		V_{IN}	-0.5 to 4.6	V
Switch terminal I/O voltage	$V_{CC}=0V$ or Switch=Off	V_S	-0.5 to 4.6	V
	Switch=On		-0.5 to $V_{CC}+0.5$	
Clump diode current	Control input	I_{IK}	-50	mA
	Switch		± 50	
Switch I/O current		I_S	50	mA
Power dissipation		P_D	200	mW
DC V_{CC}/GND current		I_{CC}/I_{GND}	± 100	mA
Storage temperature		T_{stg}	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction. Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic		Symbol	Rating	Unit
Power supply voltage		V_{CC}	2.3 to 3.6	V
Control pin input voltage (\overline{OE})		V_{IN}	0 to 3.6	V
Switch I/O voltage	$V_{CC}=0V$ or Switch=Off	V_S	0 to 3.6	V
	Switch=On		0 to V_{CC}	
Operating temperature		T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time		dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition	V _{CC} (V)	Min	Typ.	Max	Unit
Input voltage (\overline{OE})	"H" level	V _{IH}	—	2.3 to 3.6	$0.46 \times V_{CC}$	—	—	V
	"L" level	V _{IL}	—	2.3 to 3.6	—	—	$0.25 \times V_{CC}$	
Input leakage current (\overline{OE})		I _{IN}	V _{IN} = 0 to 3.6 V	2.3 to 3.6	—	—	±1.0	μA
Power-off leakage current		I _{OFF}	V _{IN} = 0 to 3.6 V	0	—	—	±5.0	μA
Off-state leakage current (switch off)		I _{SZ}	V _{IS} = 0 to V _{CC} , $\overline{OE} = V_{CC}$	2.3 to 3.6	—	—	±5.0	μA
ON resistance (Note 2)	R _{ON}	V _{IS} = 0 V, I _{IS} = 30 mA (Note 1)	3.0	—	4.5	9	Ω	
		V _{IS} = 0.4 V, I _{IS} = 30 mA (Note 1)	3.0	—	5	9.5		
		V _{IS} = 3.0 V, I _{IS} = 30 mA (Note 1)	3.0	—	11	18		
Delta R _{ON}		ΔR _{ON}	V _{IS} = 0.4 V, 1.0 V, I _{IS} = 30 mA	3.0	—	0.5	—	Ω
On-Resistance Flatness		R _{ON(flat)}	V _{IN} = 0 V to 1.0 V, I _{IS} = 30 mA	3.0	—	1.2	—	Ω
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0	3.6	—	—	2.0	μA
Increase in I _{CC} per input		ΔI _{CC}	V _{IN} = 1.8 V	3.6	—	—	10.0	μA

Note 1: All typical values are at Ta = 25°C.

Note 2: Measured by the voltage drop between D+/D- and HSD+/HSD- pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two pins.

AC Characteristics $V_{CC} = 3.3V \pm 10\%$ ($T_a = -40$ to $85^\circ C$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Typ.	Max	Unit
Propagation Delay Time (Note)	t _{pd}	C _L =5pF	3.3 ± 0.3	—	0.25	—	ns
Turn ON Time (\overline{OE} to Output)	t _{ON}	R _L =50Ω, C _L =5pF	3.3 ± 0.3	—	4	10	ns
Turn OFF Time (\overline{OE} to Output)	t _{OFF}	R _L =50Ω, C _L =5pF	3.3 ± 0.3	—	3.2	9	ns
Output skew between center port to any other port (Note)	t _{SK(O)}	C _L =5pF	3.3 ± 0.3	—	0.1	—	ns
Skew of Opposite Transitions of the same output (t _{pHL} - t _{pLH}) (Note)	t _{SK(P)}	C _L =5pF	3.3 ± 0.3	—	0.1	—	ns
Off Isolation (Non-Adjacent)	OIRR	R _T =50Ω, f=240MHz	3.3 ± 0.3	—	-27	—	dB
Crosstalk(Non-Adjacent)	XTalk	R _T =50Ω, f=240MHz	3.3 ± 0.3	—	-60	—	dB
-3dB Bandwidth	BW	R _T =50Ω, C _L =0pF	3.3 ± 0.3	—	1100	—	MHz

Note: This parameter is guaranteed by design.

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Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Control pin input capacitance (\overline{OE})	C _{IN}	V _{IN} = 0 V (Note)	3.3	4	pF
Switch terminal Off capacitance	C _{I/O}	V _{IS} = 0 V, \overline{OE} = V _{CC} (Note)	3.3	2	pF
Switch terminal On capacitance	C _{I/O}	V _{IS} = 0 V, \overline{OE} = GND (Note)	3.3	4	pF

Note: This parameter is guaranteed by design.

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AC Test Circuit Load / Waveform

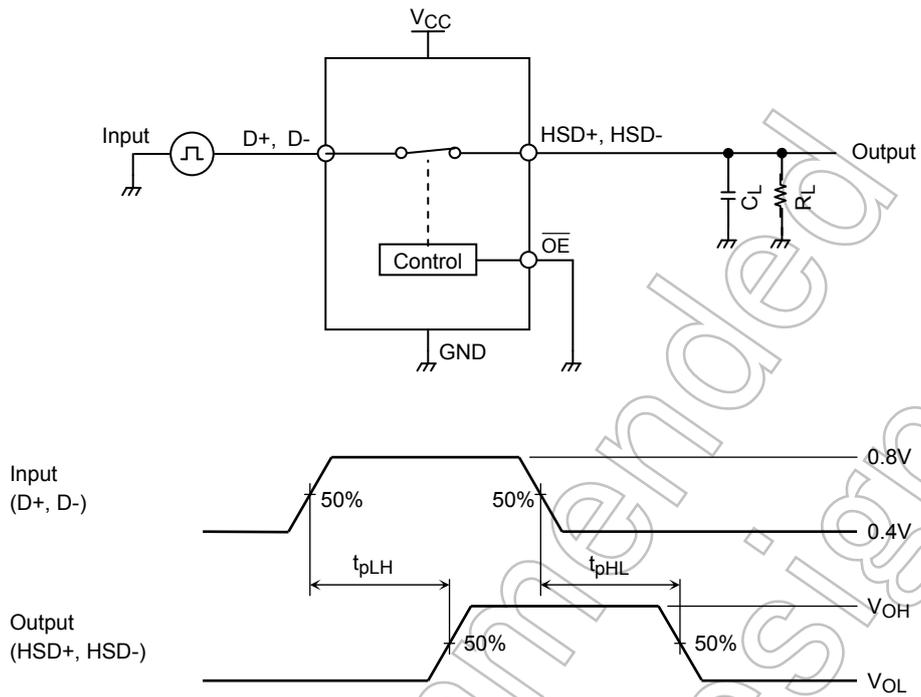


Figure 1: Propagation Delay Time (t_{pLH} , t_{pHL})

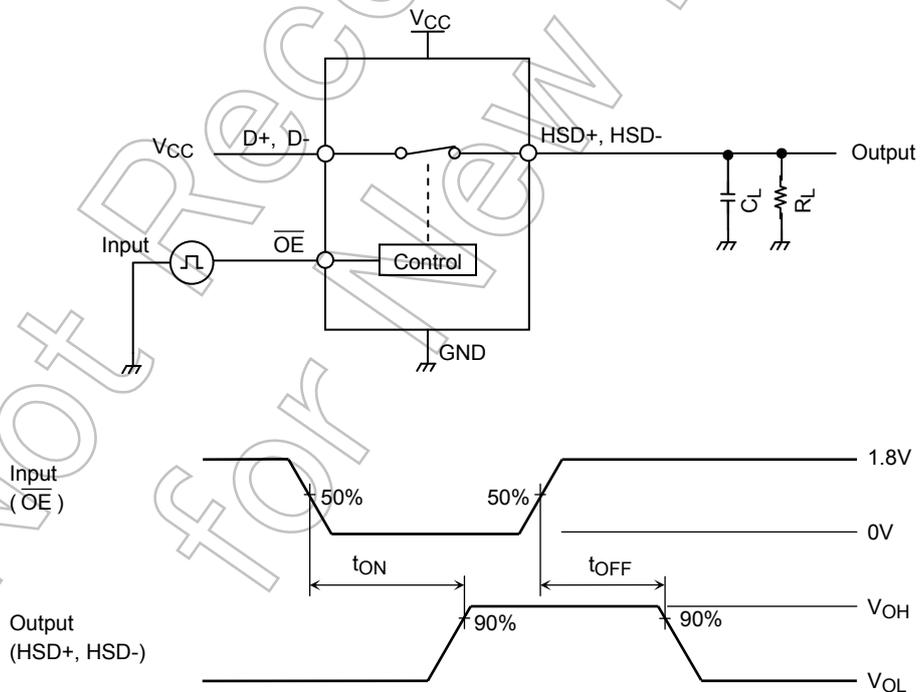


Figure 2: Turn ON/Turn OFF (t_{ON} , t_{OFF})

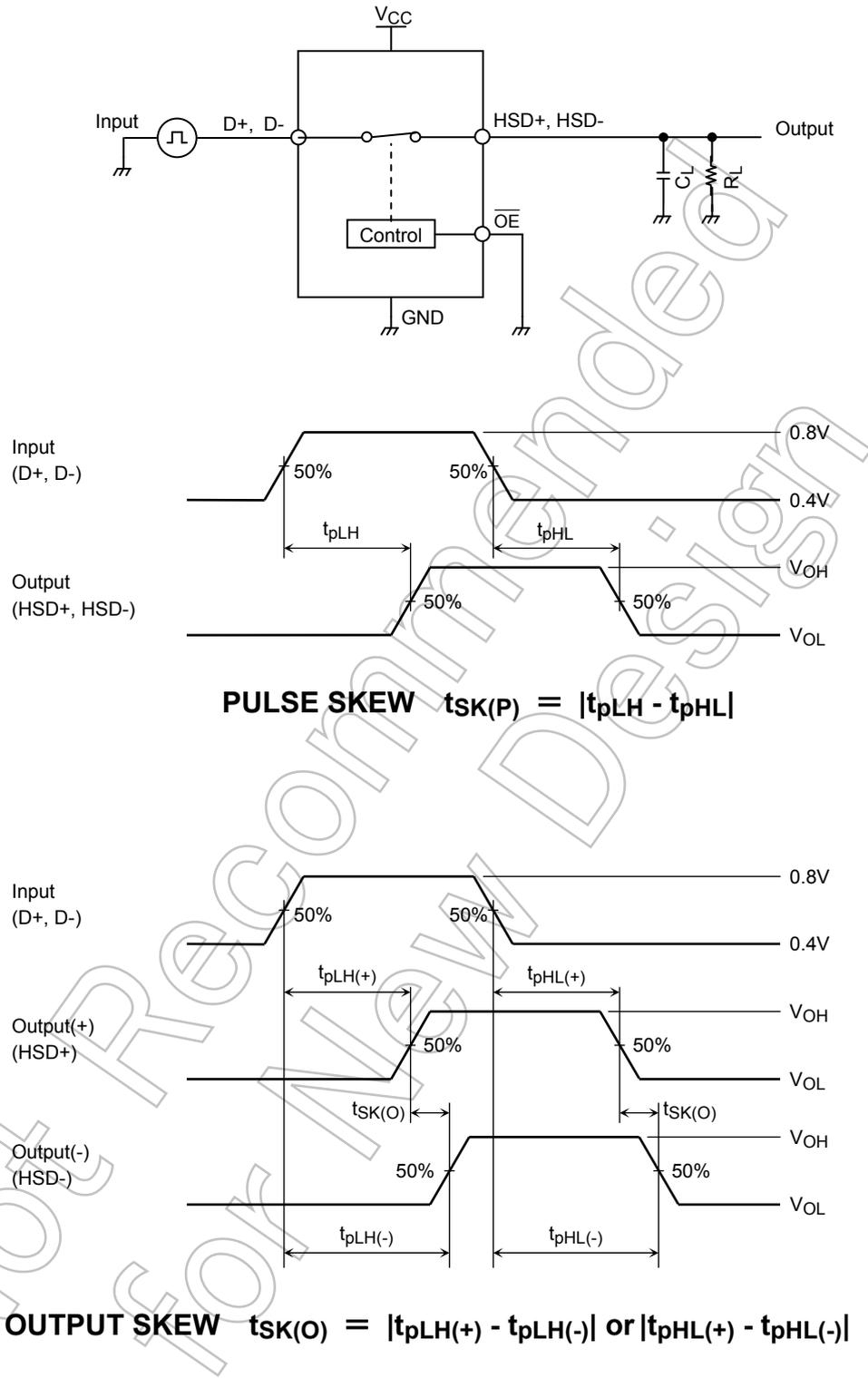


Figure 3: Skew of Opposite Transitions of the same output, Output skew

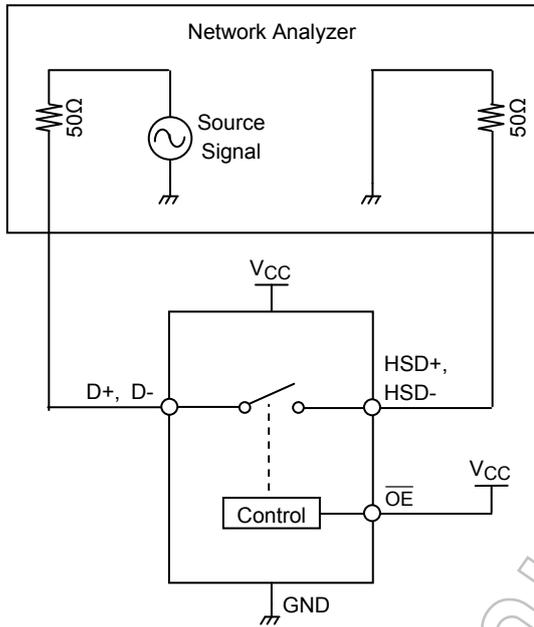


Figure 4: Channel OFF Isolation

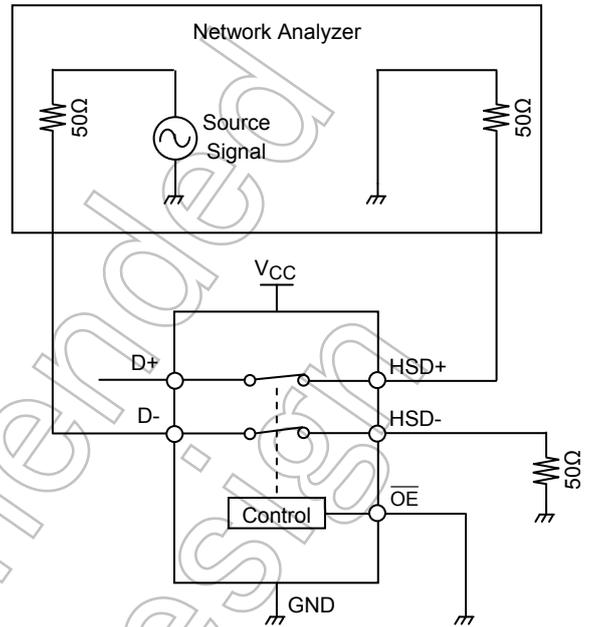


Figure 5: Crosstalk

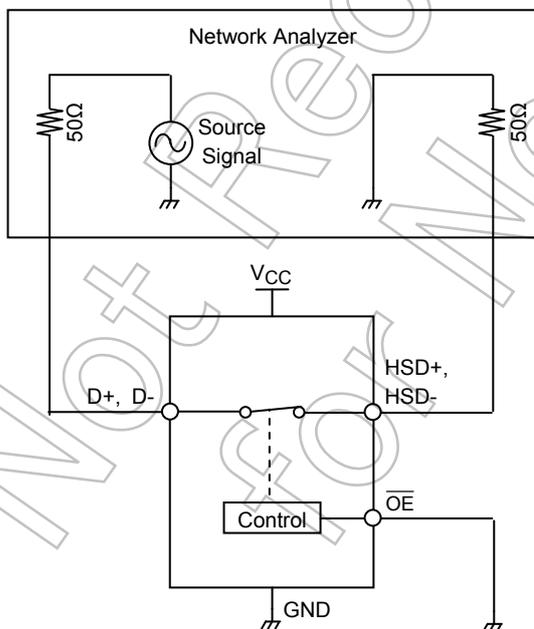


Figure 6: -3dB Bandwidth

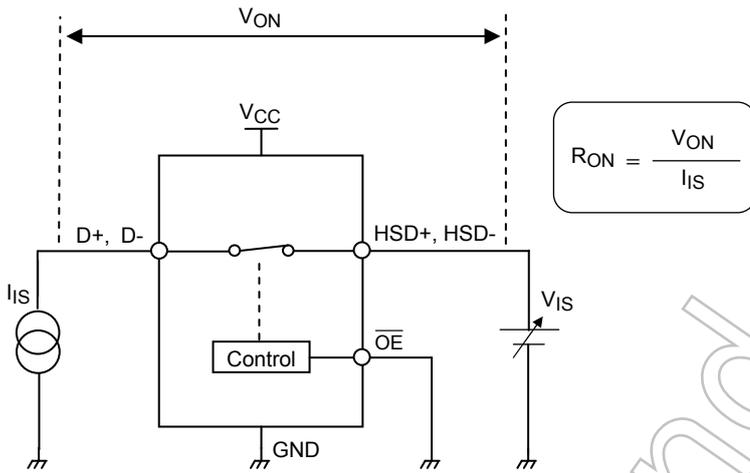


Figure 7: ON Resistance

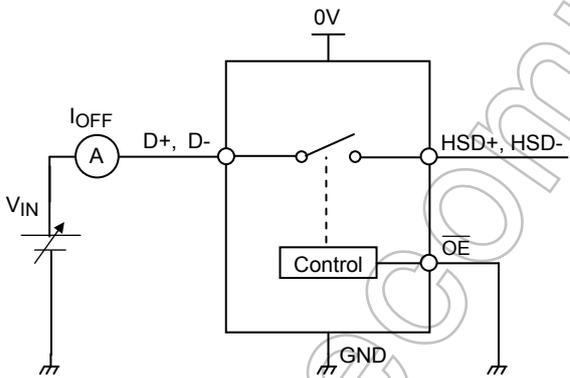


Figure 8: Power off Leakage Current

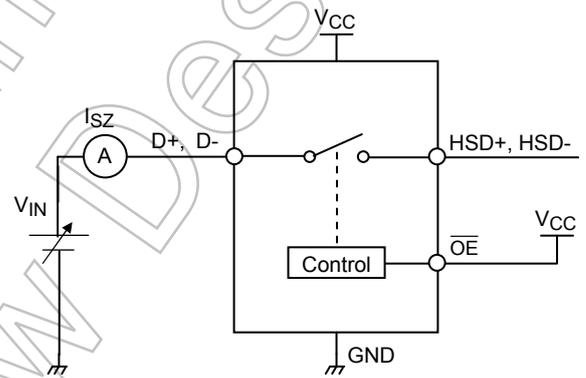


Figure 9: Off-State Leakage Current

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