

# NB6L11S

## 2.5 V 1:2 AnyLevel™ Input to LVDS Fanout Buffer / Translator

The NB6L11S is a differential 1:2 clock or data receiver and will accept AnyLevel™ input signals: LVPECL, CML, LVCMOS, LVTTTL, or LVDS. These signals will be translated to LVDS and two identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6L11S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6L11S has a wide input common mode range from  $GND + 50\text{ mV}$  to  $V_{CC} - 50\text{ mV}$ . Combined with the  $50\ \Omega$  internal termination resistors at the inputs, the NB6L11S is ideal for translating a variety of differential or single-ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6L11S is the 2.5 V version of the NB6N11S and is offered in a small 3 mm X 3 mm 16-QFN package. Application notes, models, and support documentation are available at [www.onsemi.com](http://www.onsemi.com).

### Features

- Input Clock Frequency > 2.0 GHz
- Input Data Rate > 2.5 Gb/s
- RMS Clock Jitter -0.5 ps, Typical
- 622 Mb/s Data Dependent Jitter - 6 ps, Typical
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Single Power Supply;  $V_{CC} = 2.5\text{ V} \pm 5\%$
- These are Pb-Free Devices

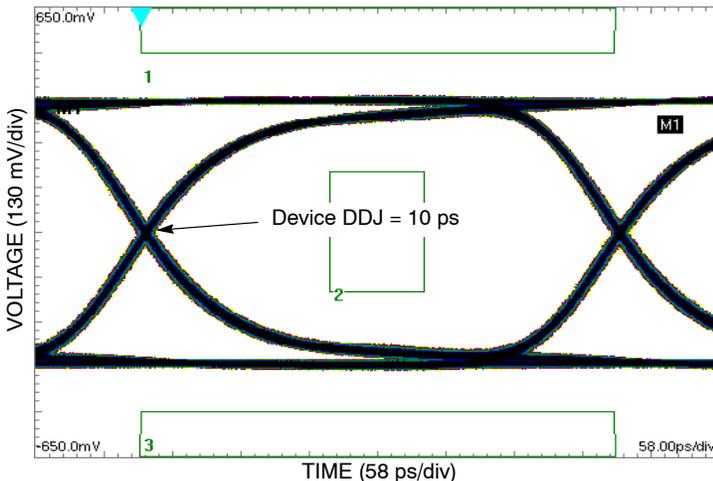


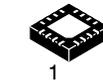
Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 400\text{ mV}$ ; Input Signal DDJ = 14 ps)



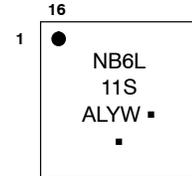
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



QFN-16  
MN SUFFIX  
CASE 485G



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

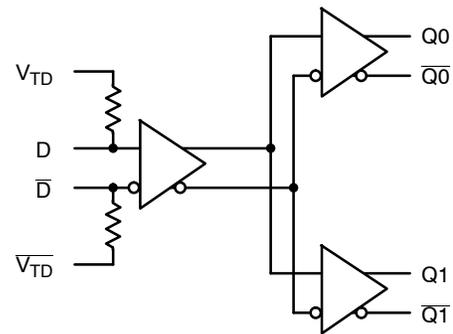


Figure 1. Logic Diagram

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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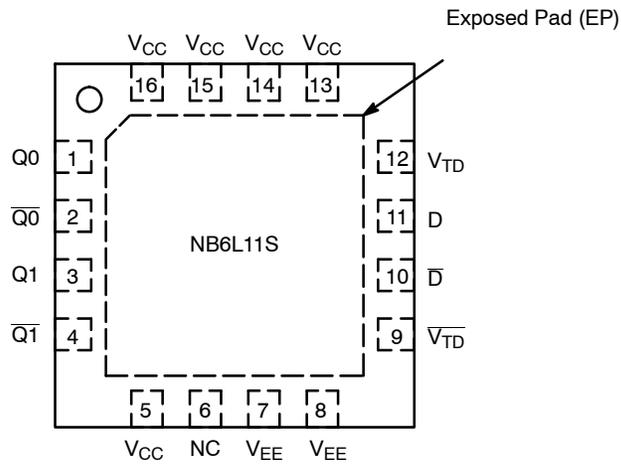


Figure 3. NB6L11S Pinout, 16-pin QFN (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q0	LVDS Output	Non-inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
2	Q0̄	LVDS Output	Inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
3	Q1	LVDS Output	Non-inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
4	Q1̄	LVDS Output	Inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
5	V <sub>CC</sub>	-	Positive Supply Voltage.
6	NC		No Connect.
7	V <sub>EE</sub>		Negative Supply Voltage.
8	V <sub>EE</sub>		Negative Supply Voltage.
9	V <sub>TD</sub> ̄	-	Internal 50 Ω termination pin for D̄.
10	D̄	LVPECL, CML, LVDS, LVCMOS, LVTTTL	Inverted Differential Clock/Data Input (Note 1).
11	D	LVPECL, CML, LVDS, LVCMOS, LVTTTL	Non-inverted Differential Clock/Data Input (Note 1).
12	V <sub>TD</sub>	-	Internal 50 Ω termination pin for D̄.
13	V <sub>CC</sub>	-	Positive Supply Voltage.
14	V <sub>CC</sub>	-	Positive Supply Voltage.
15	V <sub>CC</sub>	-	Positive Supply Voltage.
16	V <sub>CC</sub>	-	Positive Supply Voltage.
EP			Exposed pad. The exposed pad (EP) on the package bottom must be attached to a heat-sinking conduit. The exposed pad may only be electrically connected to V <sub>EE</sub> .

1. In the differential configuration when the input termination pins (V<sub>TD0</sub>/V<sub>TD0</sub>̄, V<sub>TD1</sub>/V<sub>TD1</sub>̄) are connected to a common termination voltage or left open, and if no signal is applied on D0/D0̄, D1/D1̄ input, then the device will be susceptible to self-oscillation.

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**Table 2. ATTRIBUTES**

Characteristic	Value
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 2 kV > 200 V > 1 kV
Moisture Sensitivity (Note 2)	Pb-Free Pkg
	QFN-16
	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	225
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

2. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	GND = 0 V		3.8	V
$V_{IN}$	Positive Input	GND = 0 V	$V_{IN} \leq V_{CC}$	3.8	V
$I_{IN}$	Input Current Through $R_T$ (50 $\Omega$ Resistor)	Static Surge		35 70	mA mA
$I_{OSC}$	Output Short Circuit Current Line-to-Line (Q to $\bar{Q}$ ) Line-to-End (Q or $\bar{Q}$ to GND)	Q or $\bar{Q}$ Q to $\bar{Q}$ to GND	Continuous Continuous	12 24	mA
$T_A$	Operating Temperature Range	QFN-16		-40 to +85	$^{\circ}$ C
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}$ C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-16 QFN-16	41.6 35.2	$^{\circ}$ C/W $^{\circ}$ C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	1S2P (Note 3)	QFN-16	4.0	$^{\circ}$ C/W
$T_{sol}$	Wave Solder	Pb-Free		265	$^{\circ}$ C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

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**Table 4. DC CHARACTERISTICS, CLOCK INPUTS, LVDS OUTPUTS**  $V_{CC} = 2.375 \text{ V to } 2.625 \text{ V}$ ,  $GND = 0 \text{ V}$ ,  
 $T_A = -40^\circ\text{C to } +85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{CC}$	Power Supply Current (Note 8)		30	45	mA

**DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED** (Figures 15, 16, 20, and 22)

$V_{th}$	Input Threshold Reference Voltage Range (Note 7)	GND +100		$V_{CC} - 100$	mV
$V_{IH}$	Single-ended Input HIGH Voltage	$V_{th} + 100$		$V_{CC}$	mV
$V_{IL}$	Single-ended Input LOW Voltage	GND		$V_{th} - 100$	mV

**DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (Figures 11, 12, 13, 14, 21, and 23)

$V_{IHD}$	Differential Input HIGH Voltage	100		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage	GND		$V_{CC} - 100$	mV
$V_{CMR}$	Input Common Mode Range (Differential Configuration)	GND + 50		$V_{CC} - 50$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	100		$V_{CC} - GND$	mV
$R_{TIN}$	Internal Input Termination Resistor	40	50	60	$\Omega$

**LVDS OUTPUTS** (Note 4)

$V_{OD}$	Differential Output Voltage	250		450	mV
$\Delta V_{OD}$	Change in Magnitude of $V_{OD}$ for Complementary Output States (Note 9)	0	1	25	mV
$V_{OS}$	Offset Voltage (Figure 19)	1125		1375	mV
$\Delta V_{OS}$	Change in Magnitude of $V_{OS}$ for Complementary Output States (Note 9)	0	1	25	mV
$V_{OH}$	Output HIGH Voltage (Note 5)		1425	1600	mV
$V_{OL}$	Output LOW Voltage (Note 6)	900	1075		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. LVDS outputs require 100  $\Omega$  receiver termination resistor between differential pair. See Figure 18.
5.  $V_{OHmax} = V_{OSmax} + \frac{1}{2} V_{ODmax}$ .
6.  $V_{OLmax} = V_{OSmin} - \frac{1}{2} V_{ODmax}$ .
7.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.
8. Input termination pins open, D/D at the DC level within  $V_{CMR}$  and output pins loaded with  $R_L = 100 \Omega$  across differential.
9. Parameter guaranteed by design verification not tested in production.

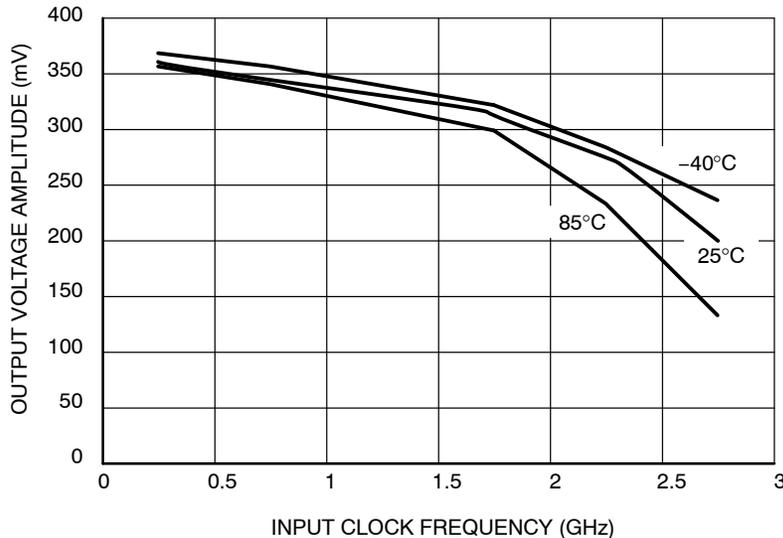
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**Table 5. AC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }2.625\text{ V}$ ,  $GND = 0\text{ V}$ ; (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) (Figure 4) $f_{in} \leq 1.0\text{ GHz}$ $f_{in} = 1.5\text{ GHz}$ $f_{in} = 2.0\text{ GHz}$	220 200 170	350 300 270		220 200 170	350 300 270		220 200 170	350 300 270		mV	
$f_{DATA}$	Maximum Operating Data Rate	1.5	2.5		1.5	2.5		1.5	2.5		Gb/s	
$t_{PLH}$ , $t_{PHL}$	Differential Input to Differential Output Propagation Delay	250		450	250	380	450	250		450	ps	
$t_{SKEW}$	Duty Cycle Skew (Note 11) Within Device Skew (Note 16) Device-to-Device Skew (Note 15)		8 5 30	45 25 100		8 5 30	45 25 100		8 5 30	45 25 100	ps	
$t_{JITTER}$	RMS Random Clock Jitter (Note 13) $f_{in} = 1.0\text{ GHz}$ $f_{in} = 1.5\text{ GHz}$ Peak-to-Peak Data Dependent Jitter (Note 14) $f_{DATA} = 622\text{ Mb/s}$ $f_{DATA} = 1.5\text{ Gb/s}$ $f_{DATA} = 2.488\text{ Gb/s}$		0.5 0.5 6 7 10			0.5 0.5 6 7 10			0.5 0.5 6 7 10		ps	
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 12)	100		$V_{CC} - GND$	100		$V_{CC} - GND$	100		$V_{CC} - GND$	mV	
$t_r$ , $t_f$	Output Rise/Fall Times @ 250 MHz (20% – 80%)	Q, $\bar{Q}$	70	120	170	70	120	170	70	120	170	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured by forcing  $V_{INPPmin}$  with 50% duty cycle clock source and  $V_{CC} - 1400\text{ mV}$  offset. All loading with an external  $R_L = 100\ \Omega$  across "D" and  $\bar{D}$  of the receiver. Input edge rates 150 ps (20%–80%).
11. See Figure 17 differential measurement of  $t_{skew} = |t_{PLH} - t_{PHL}|$  for a nominal 50% differential clock input waveform @ 250 MHz.
12. Input voltage swing is a single-ended measurement operating in differential mode.
13. RMS jitter with 50% Duty Cycle input clock signal.
14. Deterministic jitter with input NRZ data at PRBS  $2^{23}-1$  and K28.5.
15. Skew is measured between outputs under identical transition @ 250 MHz.
16. The worst case condition between  $Q0/\bar{Q}0$  and  $Q1/\bar{Q}1$  from either  $D0/\bar{D}0$  or  $D1/\bar{D}1$ , when both outputs have the same transition.



**Figure 4. Output Voltage Amplitude ( $V_{OUTPP}$ ) versus Input Clock Frequency ( $f_{in}$ ) and Temperature (@  $V_{CC} = 2.5\text{ V}$ )**

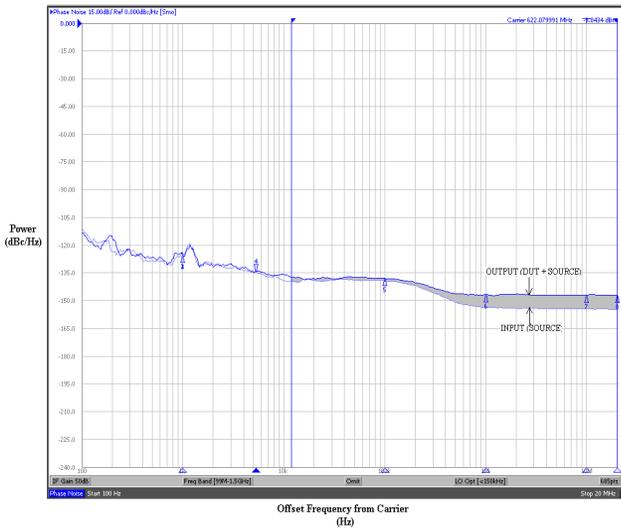


Figure 5. Typical Phase Noise Plot at  $f_{\text{carrier}} = 622.08 \text{ MHz}$

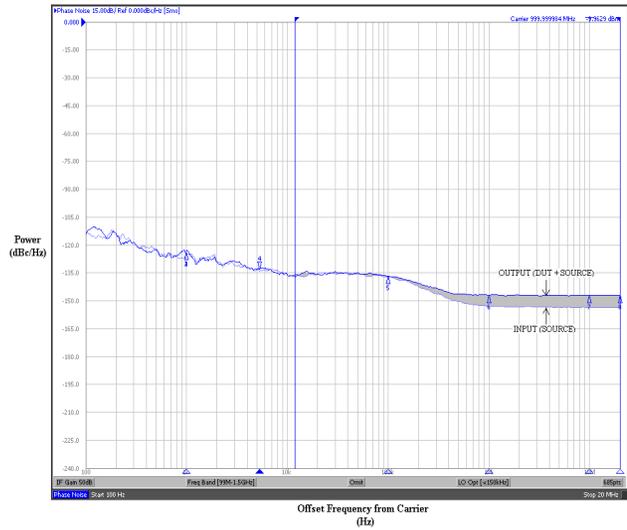


Figure 6. Typical Phase Noise Plot at  $f_{\text{carrier}} = 1 \text{ GHz}$

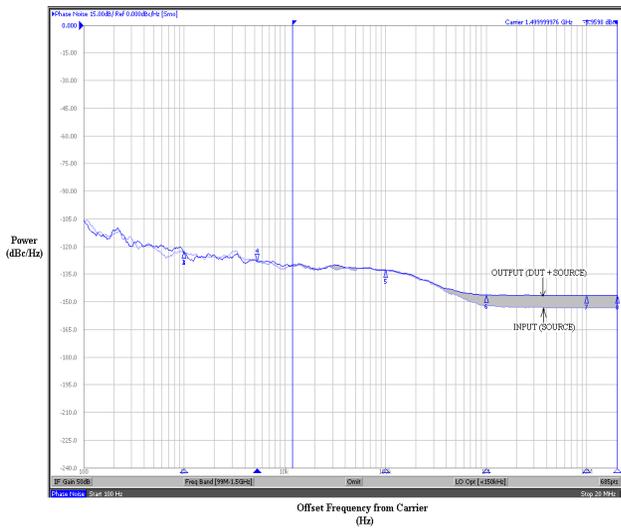


Figure 7. Typical Phase Noise Plot at  $f_{\text{carrier}} = 1.5 \text{ GHz}$

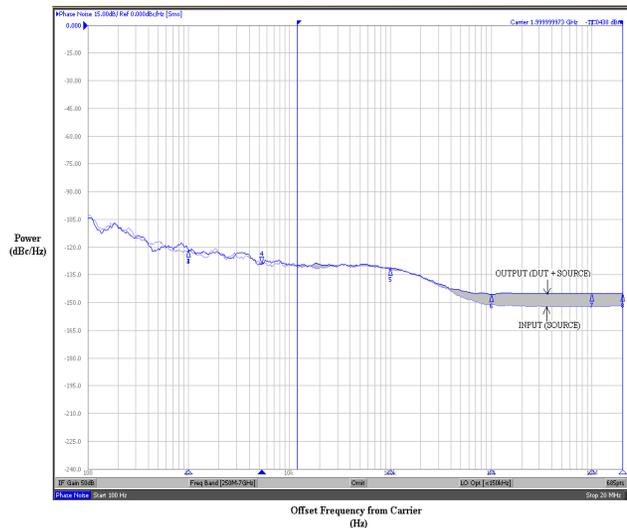


Figure 8. Typical Phase Noise Plot at  $f_{\text{carrier}} = 2 \text{ GHz}$

The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L11S device at frequencies 622.08 MHz, 1 GHz, 1.5 GHz and 2 GHz respectively at an operating voltage of 2.5 V in room temperature. The RMS Phase Jitter contributed by the

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 40 fs, 22 fs, 14 fs and 12 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.



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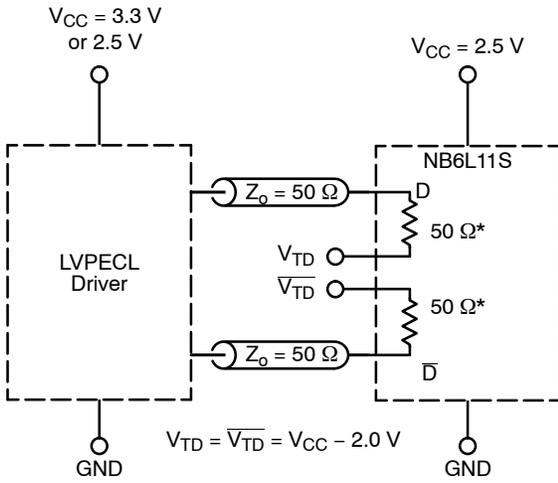


Figure 11. LVPECL Interface

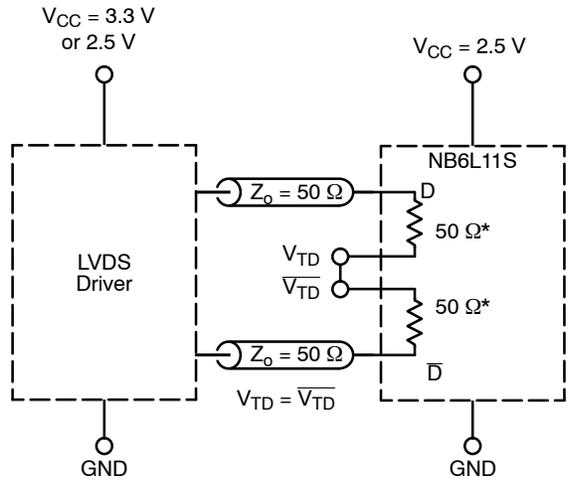


Figure 12. LVDS Interface

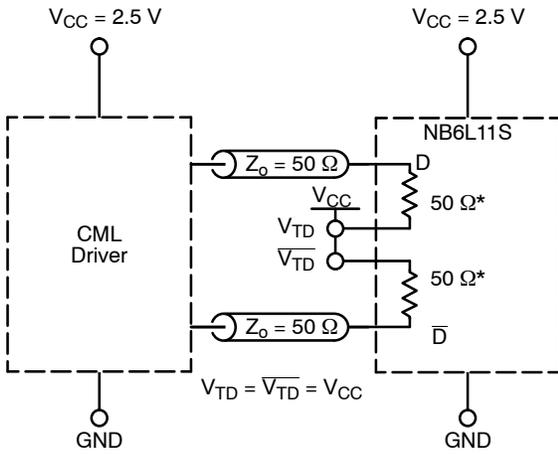


Figure 13. Standard 50  $\Omega$  Load CML Interface

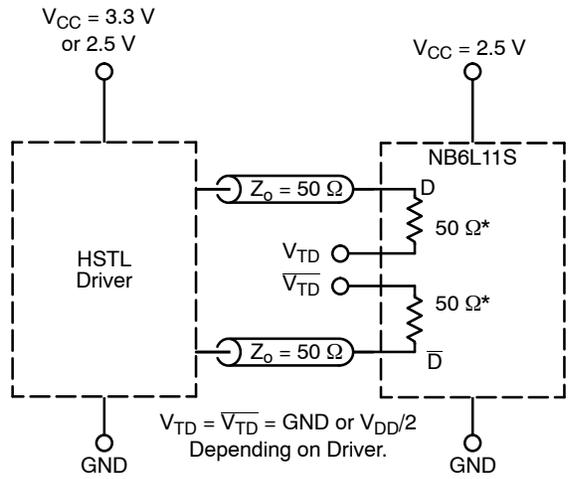


Figure 14. HSTL Interface

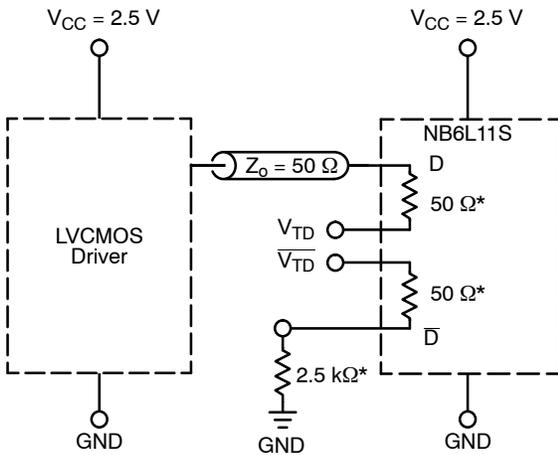


Figure 15. LVCMOS Interface

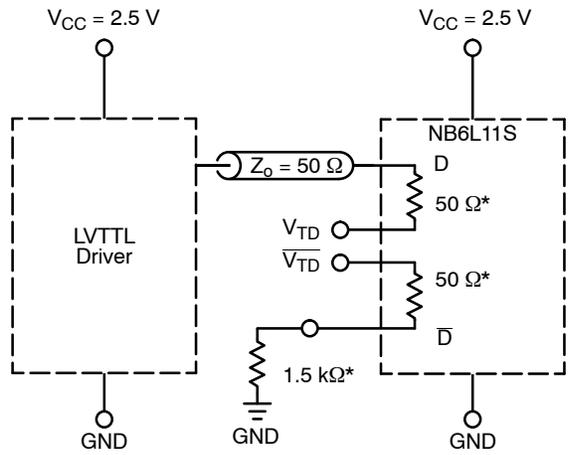


Figure 16. LVTTTL Interface

\* $R_{TIN}$ , Internal Input Termination Resistor.

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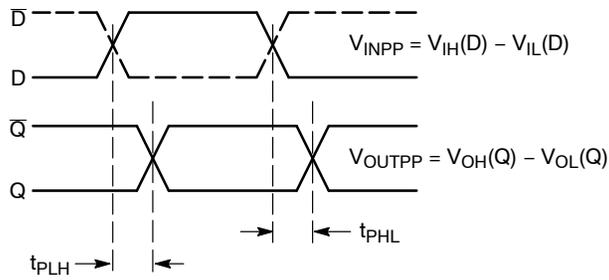


Figure 17. AC Reference Measurement

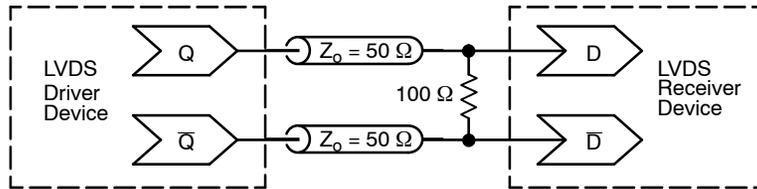


Figure 18. Typical LVDS Termination for Output Driver and Device Evaluation

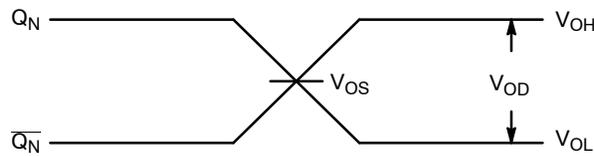


Figure 19. LVDS Output

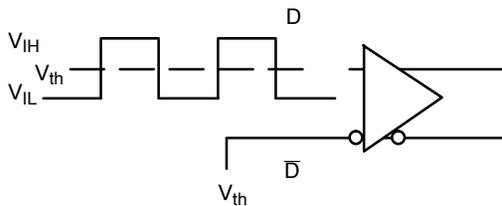


Figure 20. Differential Input Driven Single-Ended

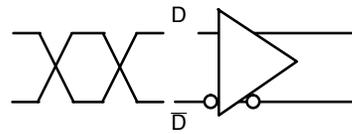


Figure 21. Differential Inputs Driven Differentially

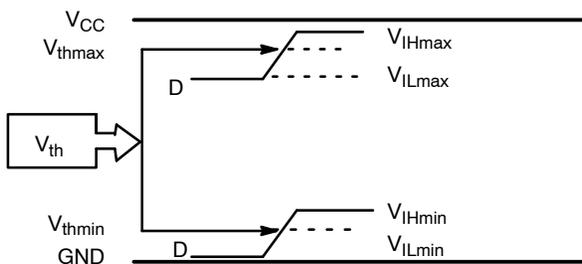


Figure 22.  $V_{th}$  Diagram

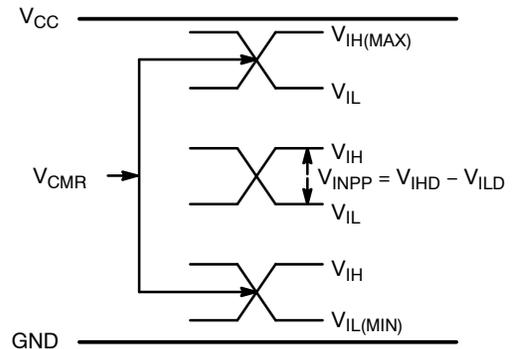


Figure 23.  $V_{CMR}$  Diagram

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## ORDERING INFORMATION

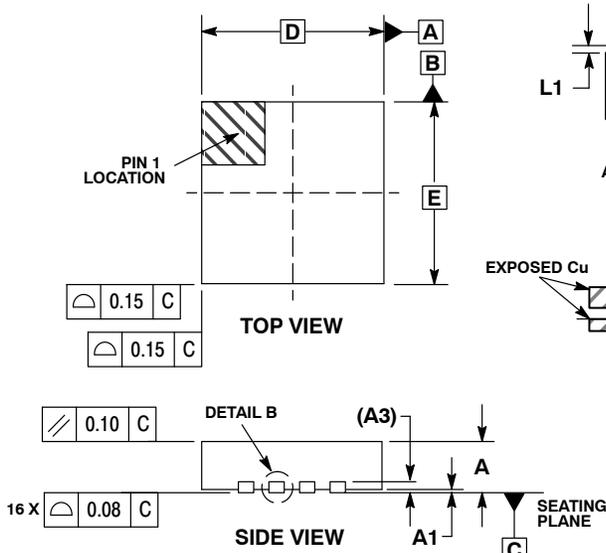
Device	Package	Shipping†
NB6L11SMNG	QFN-16, 3 X 3 mm (Pb-Free)	123 Units / Rail
NB6L11SMNR2G	QFN-16, 3 X 3 mm (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

### 16 PIN QFN CASE 485G-01 ISSUE D

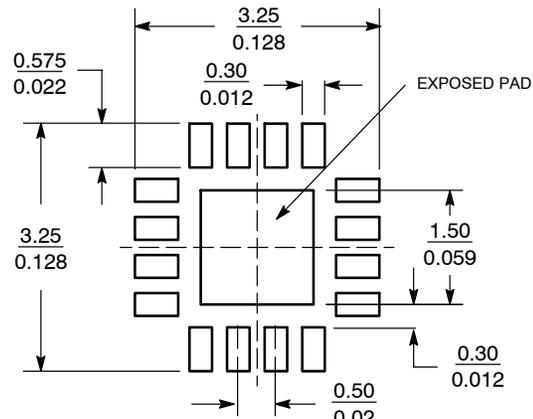
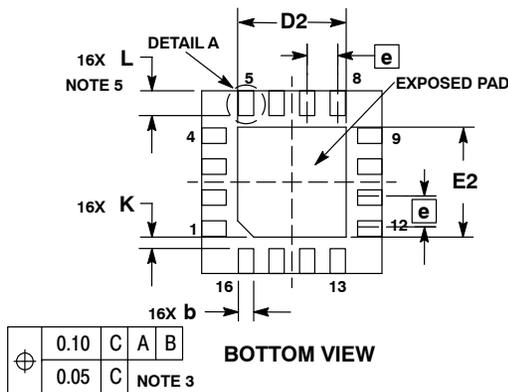


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L<sub>max</sub> CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
e	0.50	BSC
K	0.18	TYP
L	0.30	0.50
L1	0.00	0.15

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NB6L11S), may be covered by U.S. patents including 6,362,644. There may be other patents pending.

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