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December 2013

### FDH210N08

# N-Channel UniFET<sup>TM</sup> MOSFET

**75 V, 210 A, 5.5 m** $\Omega$ 

#### **Features**

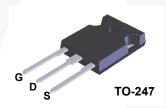
- $R_{DS(on)}$  = 4.65 m $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 125 A
- Low Gate Charge (Typ. 232 nC)
- Low C<sub>rss</sub> (Typ. 262 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability

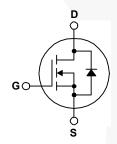
### **Applications**

- · Synchronous Rectification for ATX / Server / Telecom PSU
- · Battery Protection Circuit
- · Motor Drives and Uninterruptible Power Supplies

### **Description**

UniFET<sup>TM</sup> MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





### **Absolute Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FDH210N08	Unit	
V <sub>DSS</sub>	Drain-Source Voltage	75	V		
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		210	Α	
	- Continuous (T <sub>C</sub> = 100°C)		132	Α	
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	840	Α	
V <sub>GSS</sub>	Gate-Source Voltage		± 20	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	9375	mJ	
I <sub>AR</sub>	Avalanche Current	(Note 1)	210	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	46.2	mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns	
$P_{D}$	Power Dissipation (T <sub>C</sub> = 25°C)		462	W	
	- Derate Above 25°C		3.7	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +175	°C	
T <sub>L</sub>	MaximumLead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C		

#### **Thermal Characteristics**

Symbol	Parameter	FDH210N08	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.27	°C/W	
$R_{\theta JA}$	R <sub>0JA</sub> Thermal Resistance, Junction-to-Ambient, Max.		°C/W	

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDH210N08	FDH210N08	TO-247	Tube	N/A	N/A	30 units

## **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Charac	teristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	75			V
$\Delta BV_{DSS}$ / $\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C		0.1		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V			20	μА
		$V_{DS} = 60 \text{ V}, T_{J} = 150^{\circ}\text{C}$			250	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			200	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-200	nA
On Charac	teristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 125 A		4.65	5.5	mΩ
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 125 A		200		S
Dynamic C	Characteristics					I.
C <sub>iss</sub>	Input Capacitance			8743	11340	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0  MHz		2134	2778	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 = 1.0 WILIZ	\	262	393	pF
Switching	Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time			100	210	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 37.5 \text{ V}, I_D = 69 \text{ A},$		410	830	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$R_{G} = 25 \Omega$		630	1270	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		290	590	ns
Q <sub>q</sub>	Total Gate Charge			232	301	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{DS} = 60 \text{ V}, I_{D} = 125 \text{ A},$		58		nC
Q <sub>gd</sub>	Gate-Drain Charge	$V_{GS} = 10 \text{ V}$ (Note 4)	/	77	/	nC
Drain-Sour	rce Diode Characteristics and Maximum Rat	ings		ı		
I <sub>S</sub> Maximum Continuous Drain-Source Diode Forwa		rward Current			210	Α
I <sub>SM</sub> Maximum Pulsed Drain-Source Diode Forward		d Current			840	Α
JIVI		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 125 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V, } I_{S} = 125 \text{ A,}$		123		ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100 \text{ A/}\mu\text{s}$		420	//	nC

<sup>1.</sup> Repetitive rating: pulse-width limited by maximum junction temperature.

<sup>2.</sup>L = 0.4 mH,  $I_{AS}$  = 125 A,  $V_{DD}$  = 50 V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C. 3.  $I_{SD}$   $\leq$  125 A, di/dt  $\leq$  260 A/ $\mu$ s,  $V_{DD}$   $\leq$  BV $_{DSS}$ , starting  $T_{J}$  = 25°C.

<sup>4.</sup> Essentially independent of operating temperature typical characteristics.

### **Typical Performance Characteristics**

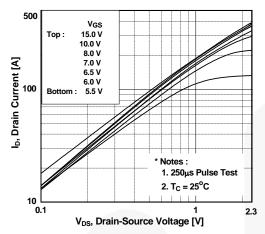


Figure 1. On-Region Characteristics

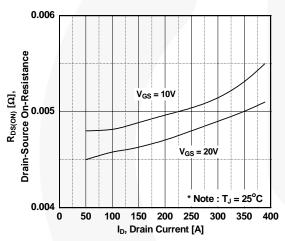


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

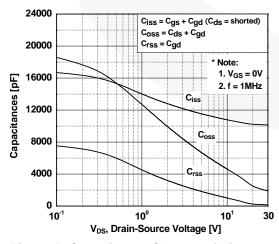


Figure 5. Capacitance Characteristics

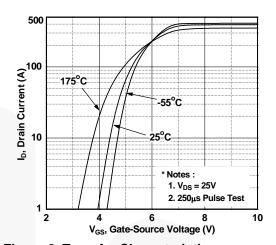


Figure 2. Transfer Characteristics

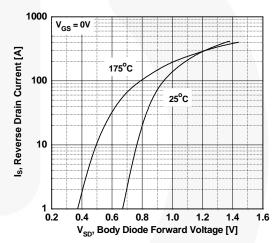


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

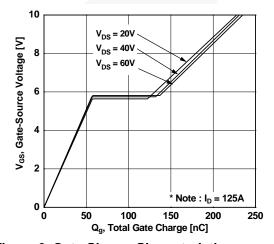


Figure 6. Gate Charge Characteristics

### **Typical Performance Characteristics** (Continued)

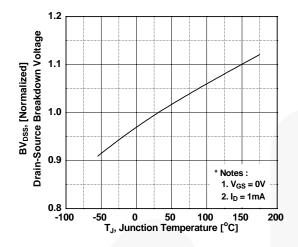


Figure 7. Breakdown Voltage Variation vs. Temperature

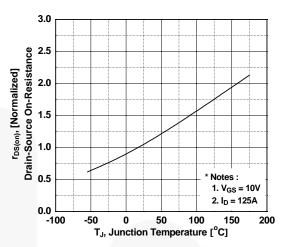


Figure 8. On-Resistance Variation vs. Temperature

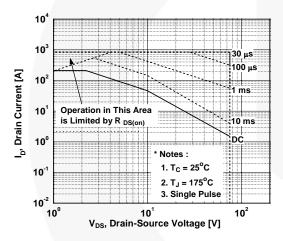


Figure 9. Maximum Safe Operating Area

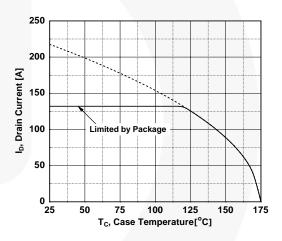


Figure 10. Maximum Drain Current vs. Case Temperature

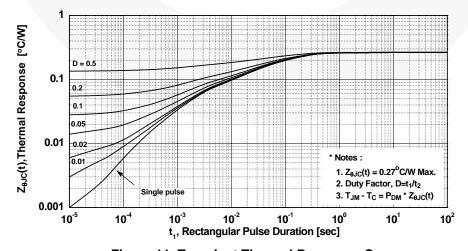


Figure 11. Transient Thermal Response Curve

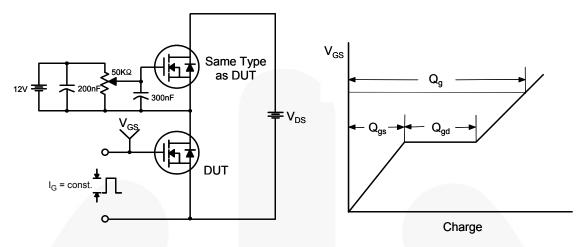


Figure 12. Gate Charge Test Circuit & Waveform

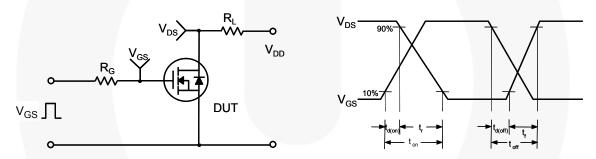


Figure 13. Resistive Switching Test Circuit & Waveforms

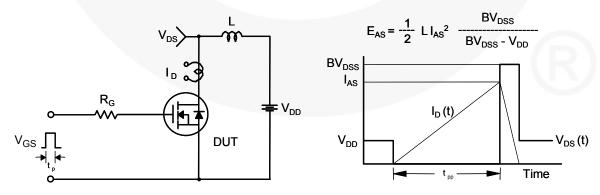


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

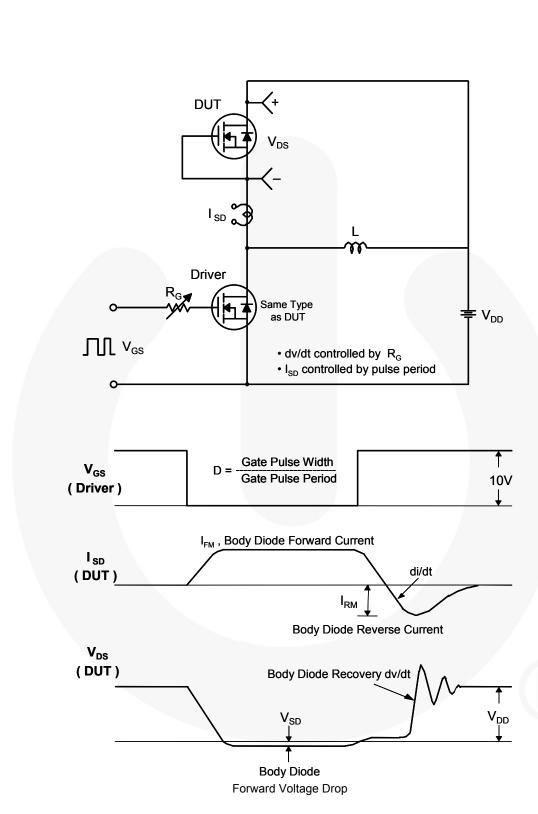


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**

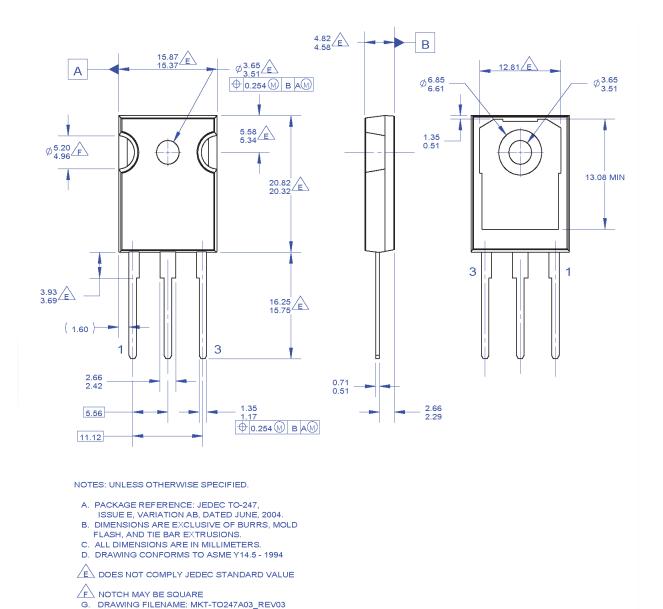


Figure 16. TO-247, Molded, 3-Lead, Jedec Variation AB

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