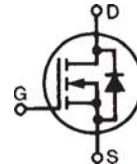


High Voltage MOSFET

N-Channel, Enhancement Mode

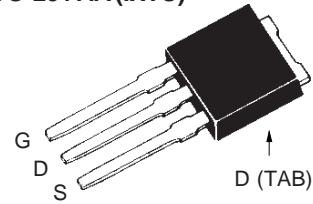
IXTU 01N100
IXTY 01N100

V_{DSS} = 1000 V
 I_{D25} = 100mA
 $R_{DS(on)}$ = 80 Ω

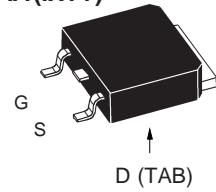


Symbol	Test Conditions	Maximum Ratings 01N100		
V_{DSS}	T_J = 25°C to 150°C	1000		V
V_{DGR}	T_J = 25°C to 150°C; $R_{GS} = 1 \text{ M}\Omega$	1000		V
V_{GS}	Continuous	± 20		V
V_{GSM}	Transient	± 30		V
I_{D25}	$T_c = 25^\circ\text{C}; T_j = 25^\circ\text{C} \text{ to } 150^\circ\text{C}$	100		mA
I_{DM}	$T_c = 25^\circ\text{C}$, pulse width limited by max. T_j	400		mA
P_D	$T_c = 25^\circ\text{C}$	25		W
T_J		-55 ... +150		°C
T_{JM}		150		°C
T_{stg}		-55 ... +150		°C
T_L	1.6 mm (0.063 in) from case for 5 s	300		°C
Weight		0.8		g

TO-251 AA (IXTU)



TO-252 AA (IXTY)



G = Gate,
S = Source,
D = Drain,
TAB = Drain

Symbol	Test Conditions	Characteristic Values		
		($T_j = 25^\circ\text{C}$, unless otherwise specified)	min.	typ.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 25 \mu\text{A}$	1000		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 25 \mu\text{A}$	2		4.5 V
I_{GSS}	$V_{GS} = \pm 20 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 50 \text{ nA}$
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0 \text{ V}$	$T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$		10 μA 200 μA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = I_{D25}$ Pulse test, $t \leq 300 \text{ ms}$, duty cycle $d \leq 2 \%$	60	80	Ω

Features

- International standard packages JEDEC TO-251 AA, TO-252 AA
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Fast switching times

Applications

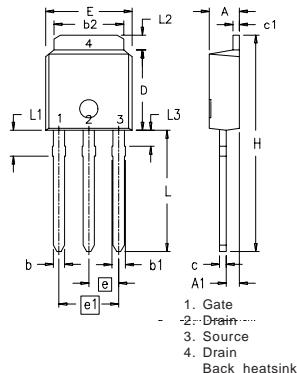
- Level shifting
- Triggers
- Solid state relays
- Current regulators

Symbol **Test Conditions**
Characteristic Values
 $(T_J = 25^\circ\text{C}, \text{unless otherwise specified})$
min. **typ.** **max.**

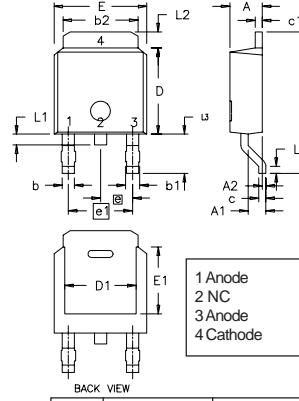
g_{fs}	$V_{DS} = 10 \text{ V}; I_D = 0.5 \cdot I_{D25}$, pulse test	160	mS
C_{iss} C_{oss} C_{rss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	54	pF
		6.9	pF
		2	pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	$V_{GS} = 10 \text{ V}, V_{DS} = 500 \text{ V}, I_D = I_{D25}$ $R_G = 50 \Omega$ (External)	12	ns
		12	ns
		28	ns
		28	ns
$Q_{g(on)}$ Q_{gs} Q_{gd}	$V_{GS} = 10 \text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 I_{D25}$	6.9	nC
		1.8	nC
		3.0	nC
R_{thJC}		5	K/W

Source-Drain Diode
Characteristic Values
 $(T_J = 25^\circ\text{C}, \text{unless otherwise specified})$
Symbol **Test Conditions**
min. **typ.** **max.**

V_{SD}	$I_F = 100 \text{ mA}, V_{GS} = 0 \text{ V}$, Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2 \%$	1.8	V
t_{rr}	$I_F = 0.75 \text{ A}, -di/dt = 10 \text{ A}/\mu\text{s}$, $V_{DS} = 25 \text{ V}$	1.5	μs

TO-251 AA Outline


Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	2.19	2.38	.086	.094
A1	0.89	1.14	.035	.045
b	0.64	0.89	.025	.035
b1	0.76	1.14	.030	.045
b2	5.21	5.46	.205	.215
c	0.46	0.58	.018	.023
c1	0.46	0.58	.018	.023
D	5.97	6.22	.235	.245
E	6.35	6.73	.250	.265
e	2.28	BSC	.090	BSC
e1	4.57	BSC	.180	BSC
H	17.02	17.78	.670	.700
L	8.89	9.65	.350	.380
L1	1.91	2.28	.075	.090
L2	0.89	1.27	.035	.050
L3	1.15	1.52	.045	.060

TO-252 AA


Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	2.54	2.92	0.100	0.115

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

 4,835,592 4,881,106 5,017,508
 4,850,072 4,931,844 5,034,796

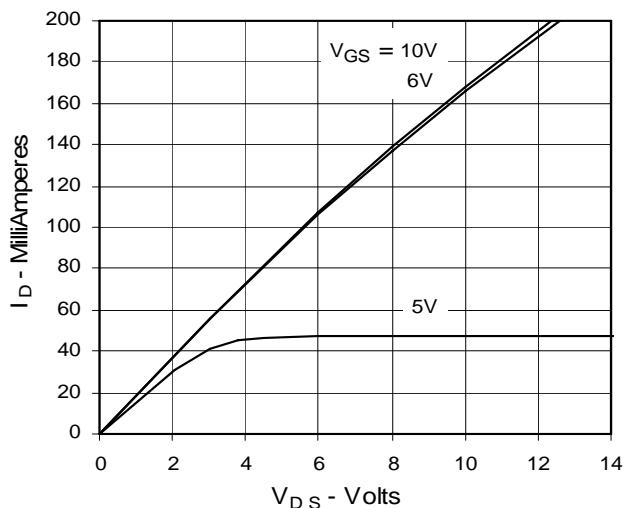
 5,049,961
 5,063,307

 5,187,117
 5,237,481

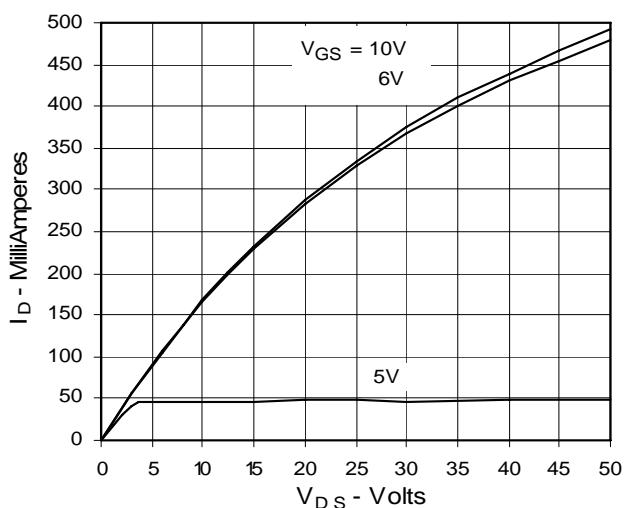
 5,486,715
 5,381,025

6,306,728B1

**Fig. 1. Output Characteristics
@ 25°C**



**Fig. 2. Extended Output Characteristics
@ 25°C**



**Fig. 3. Output Characteristics
@ 125°C**

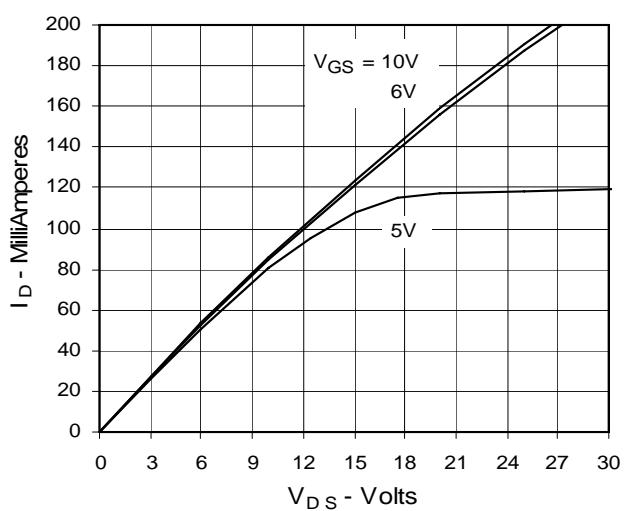
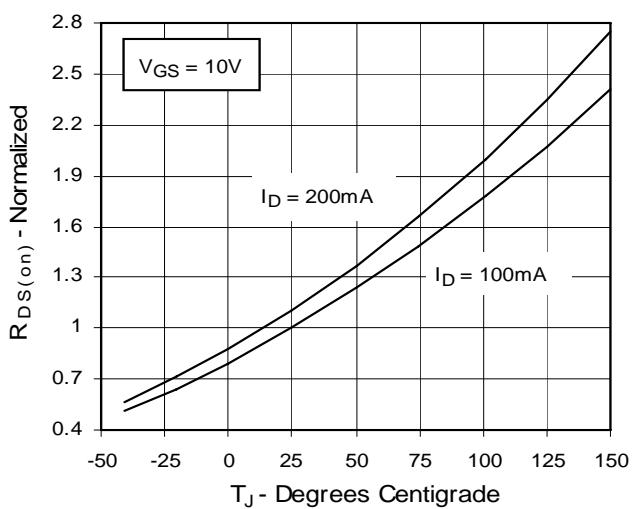


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature



**Fig. 5. $R_{DS(on)}$ Normalized to
0.5 I_{D25} Value vs. I_D**

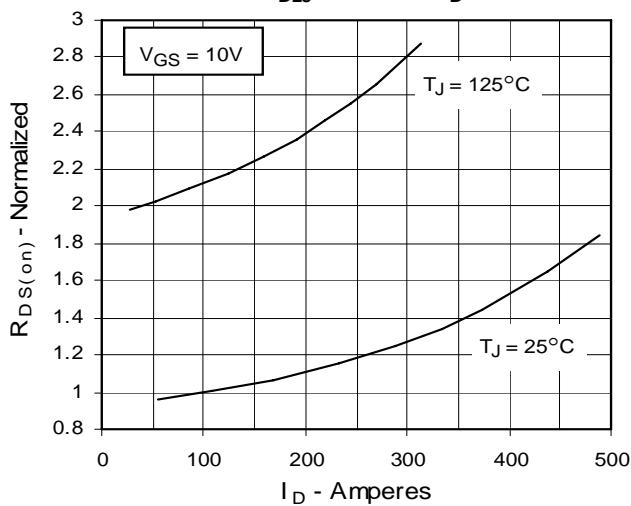


Fig. 6. Drain Current vs. Case Temperature

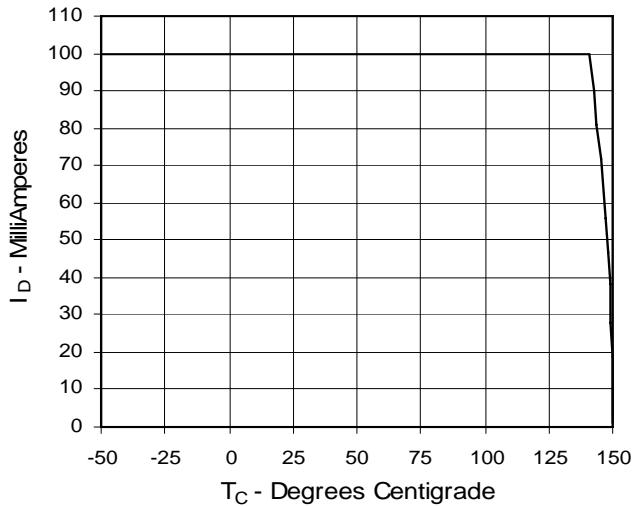
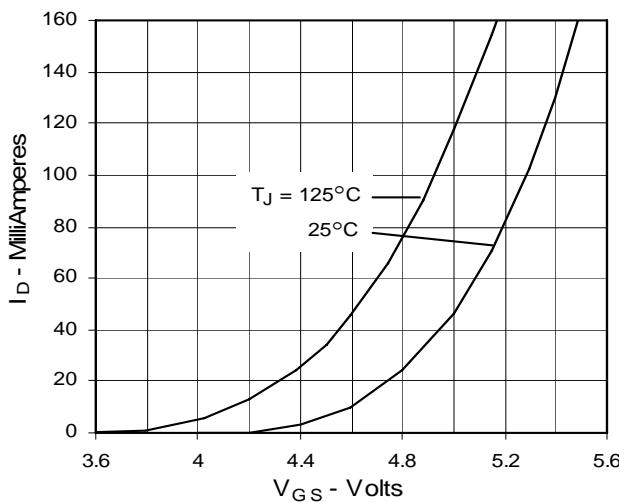
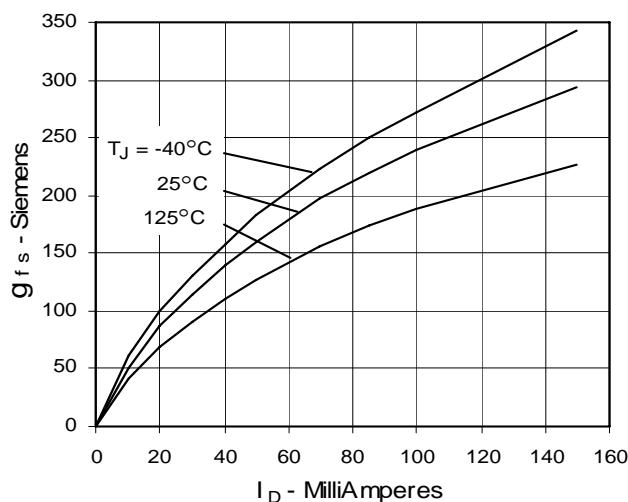
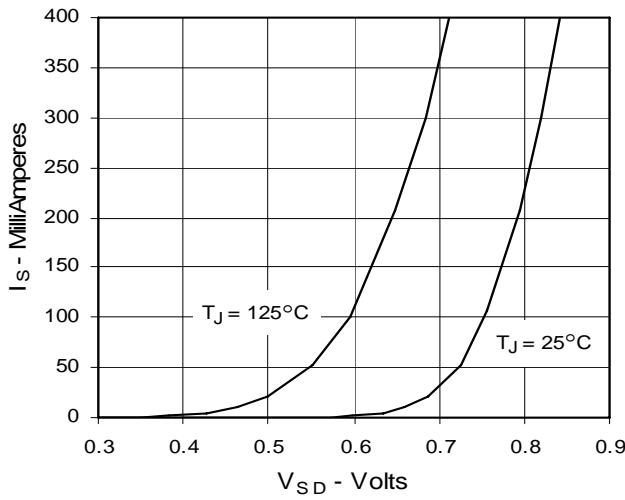
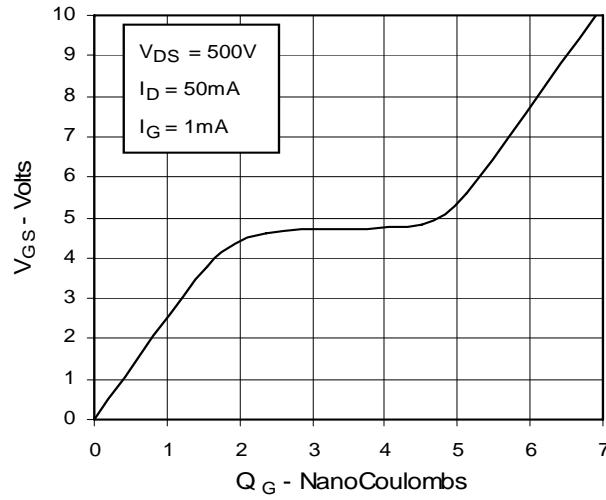
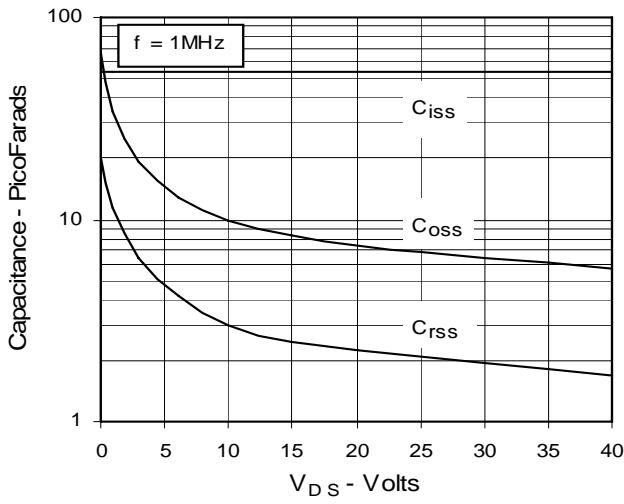
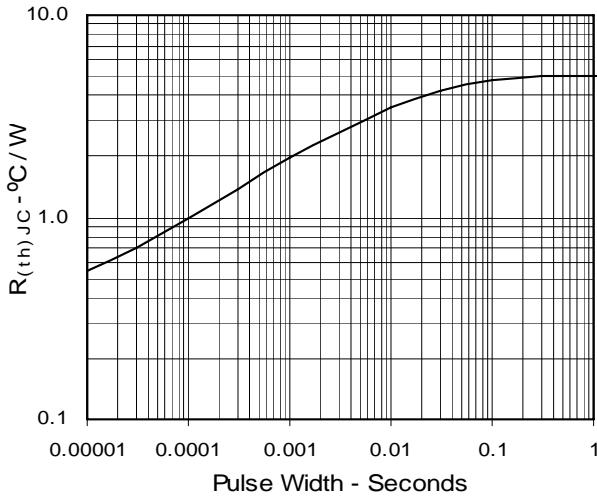


Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Source Current vs. Source-To-Drain Voltage

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Maximum Transient Thermal Resistance


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