

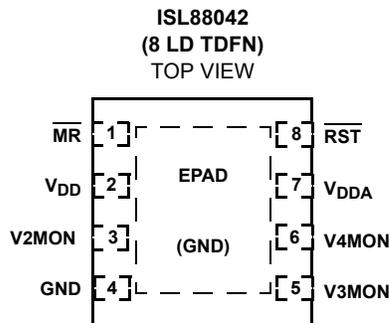
## Quadruple Voltage Monitor

The ISL88042 is a Quadruple voltage-monitoring supervisor combining competitive reset threshold accuracy and low power consumption. This device combines popular functions such as Power-On Reset, Undervoltage Supply Supervision, reset signaling and Manual Reset. Monitoring four different supplies in a 8 Ld 2x3 TDFN package, the ISL88042 devices can help to lower system cost, reduce board space requirements, and increase the reliability of multi-voltage systems.

Low  $V_{DD}$  detection circuitry protects the user's system from low voltage conditions, resetting the system when  $V_{DD}$  or any of the other monitored power supply voltages fall below their respective minimum voltage thresholds. The reset signal remains asserted until all of these voltages return to proper operating levels and stabilize.

Two of the four voltage monitors have preset thresholds for either dual 3.3V or one each for one 5V and one 3.3V supplies. Users can adjust the threshold voltages of the third and fourth voltage monitors in order to meet specific system level requirements.

## Pinout



## Features

- Quadruple Voltage Monitoring
- Fixed-Voltage Options Allow Precise Monitoring of +5.0V and +3.3V Power Supplies
- Two Adjustable Voltage Inputs Monitor Voltages > 0.6V
- 95ms Nominal Reset Pulse Width
- Manual Reset Capability
- Reset Signals Valid Down to  $V_{DD} = 1V$
- Immune to Power-Supply Transients
- Low 22 $\mu$ A Maximum Supply Current at 5V
- Pb-Free (RoHS Compliant)

## Applications

- Telecom and Datacom Systems
- Routers and Servers
- Access Concentrators
- Cable/Satellite Applications
- Desktop and Notebook Computer Systems
- Data Storage Equipment
- Set-Top Boxes
- Industrial Equipment
- Multi-Voltage Systems

## Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	$V_{TH1}$ (V)	$V_{TH2}$ (V)	TEMP RANGE (°C)	PACKAGE Tape & Reel (Pb-free)	PKG. DWG. #
ISL88042IRTHFZ-T	4P6	4.60	3.09	-40 to +85	8 Ld TDFN	L8.2x3A
ISL88042IRTHFZ-TK	4P6	4.60	3.09	-40 to +85	8 Ld TDFN	L8.2x3A
ISL88042IRTEEZ-T	2P9	2.87	2.95	-40 to +85	8 Ld TDFN	L8.2x3A
ISL88042IRTEEZ-TK	2P9	2.87	2.95	-40 to +85	8 Ld TDFN	L8.2x3A
ISL88042IRTJJZ-T	2P8	2.78	2.86	-40 to +85	8 Ld TDFN	L8.2x3A
ISL88042IRTJJZ-TK	2P8	2.78	2.86	-40 to +85	8 Ld TDFN	L8.2x3A

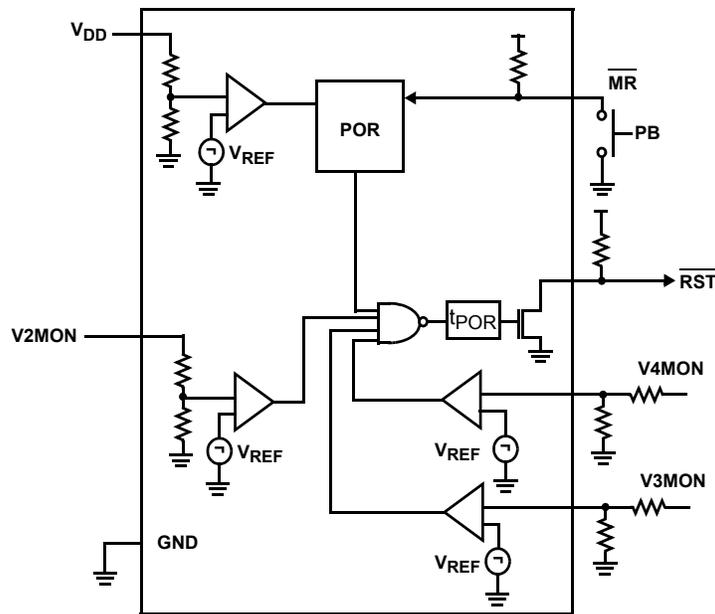
### NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Pin Descriptions**

ISL88042 PIN NUMBER	PIN NAME	FUNCTION
1	$\overline{\text{MR}}$	Active-Low open drain manual reset input with internal pull-up resistor
2	$V_{\text{DD}}$	Chip Bias Input and primary integrated preset undervoltage monitor
3	V2MON	Secondary integrated preset undervoltage monitor input
4	GND	Ground
5	V3MON	Adjustable undervoltage monitor input
6	V4MON	Adjustable undervoltage monitor input
7	$V_{\text{DDA}}$	Must be tied to $V_{\text{DD}}$ for proper operation
8	$\overline{\text{RST}}$	Active-low open drain reset output

**Functional Block Diagram**



**Absolute Maximum Ratings**

Temperature Under Bias	-40°C to +125°C
Voltage on VDD with Respect to GND	-1.0V to +7V
Voltage on V3MON, V4MON	-1.0V to 3V
Voltage on Any Other Pin	-1.0V to VDD + 0.3V
DC Output Current	5mA

**Thermal Information**

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
8 Ld TDFN Package (Notes 3, 4)	60	8
Pb-free Reflow Profile	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

**Recommended Operating Conditions**

Operating Temperature Range (Industrial)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTE:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
- For  $\theta_{JC}$ , the “case temp” location is the center of the exposed metal pad on the package underside.

**Electrical Specifications** Over the recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
V <sub>DD</sub>	Supply Voltage Range		2.0		5.5	V
I <sub>DD1</sub>	V <sub>DD</sub> Supply Current	V <sub>DD</sub> = 5.0V		14	22	μA
I <sub>DD2</sub>	V2MON Input Current	V2MON = 3.3V		5.5	8	μA
I <sub>DDA</sub>	V3MON, V4MON Input Current	V3MON, V4MON = 1.0V		19	100	nA
<b>VOLTAGE THRESHOLDS</b>						
V <sub>TH1</sub>	Fixed Voltage Trip Point for V <sub>DD</sub>	ISL88042IRTHFZ	4.370	4.600	4.830	V
		ISL88042IRTEEZ	2.734	2.872	3.010	V
		ISL88042IRTJJZ	2.647	2.780	2.914	V
V <sub>TH1HYST</sub>	Hysteresis of V <sub>TH1</sub>	V <sub>TH1</sub> = 4.60V		92		mV
		V <sub>TH1</sub> = 2.87V		58		mV
		V <sub>TH1</sub> = 2.78V		58		mV
V <sub>TH2</sub>	Fixed Voltage Trip Point for V2MON	ISL88042IRTHFZ	2.936	3.090	3.245	V
		ISL88042IRTEEZ	2.815	2.957	3.099	V
		ISL88042IRTJJZ	2.725	2.860	3.000	V
V <sub>TH2HYST</sub>	Hysteresis of V <sub>TH2</sub>	V <sub>TH2</sub> = 3.09V		61		mV
		V <sub>TH2</sub> = 2.96V		60		mV
		V <sub>TH2</sub> = 2.86V		60		
V <sub>REF</sub>	ISL88042IRTHFZ, ISL88042IRTEEZ Adj. Reset Threshold Voltage	V <sub>TH</sub> for V3MON, V4MON	0.572	0.600	0.630	V
V <sub>REF</sub>	ISL88042IRTJJZ Adj. Reset Threshold Voltage	V <sub>TH</sub> for V3MON, V4MON	0.554	0.581	0.610	V
V <sub>REFHYST</sub>	Hysteresis Voltage			12		mV
<b>RESET</b>						
V <sub>OL</sub>	Reset Output Voltage Low	V <sub>DD</sub> ≥ 3.3V, Sinking 2.5mA		0.05	0.40	V
		V <sub>DD</sub> < 3.3V, Sinking 1.5mA		0.05	0.40	V
t <sub>RPD</sub>	V <sub>TH</sub> to Reset Asserted Delay			6		μs
t <sub>POR</sub>	POR Timeout Delay	V3MON, V4MON < 3V	40	95	150	ms

**Electrical Specifications** Over the recommended operating conditions, unless otherwise specified. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
<b>MANUAL RESET</b>						
V <sub>MRL</sub>	$\overline{\text{MR}}$ Input Voltage Low				0.8	V
V <sub>MRH</sub>	$\overline{\text{MR}}$ Input Voltage High		V <sub>DD</sub> - 0.6			V
t <sub>MR</sub>	$\overline{\text{MR}}$ Minimum Pulse Width		550			ns
R <sub>PU</sub>	Internal Pull-Up Resistor			10		kΩ

NOTE:

- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

**Pin Descriptions**

**$\overline{\text{RST}}$**

The  $\overline{\text{RST}}$  output is an open drain output, which is asserted low whenever the following occurs:

- The device is initially powered up to 1V or
- V<sub>DD</sub>, V2MON, V3MON or V4MON fall below their minimum voltage sense level.

**$\overline{\text{MR}}$**

The  $\overline{\text{MR}}$  input is an active low debounced input to which a user can connect a push-button to add manual reset capability or use a signal to pull low.  $\overline{\text{MR}}$  has an internal pull-up resistor.

**V<sub>DD</sub>**

The V<sub>DD</sub> pin is the IC power supply terminal. The voltage at this pin is compared against an internal factory-programmed voltage trip point, V<sub>TH1</sub>.  $\overline{\text{RST}}$  is first asserted low when the device is initially powered and V<sub>DD</sub> < 1V and then at any time thereafter when V<sub>DD</sub> falls below V<sub>TH1</sub>. The device is designed with hysteresis to help prevent chattering due to noise and is immune to brief power-supply transients.

**V2MON**

The V2MON input is the second preset monitored voltage that causes the  $\overline{\text{RST}}$  output to go low when the voltage on V2MON falls below V<sub>TH2</sub>.

**V3MON, and V4MON**

The VxMON inputs provide monitoring and UV compliance of three additional voltages through resistor dividers. A reset is issued on the ISL88042 if the voltage on any VxMON falls below the internal V<sub>REF</sub> of 0.6V.

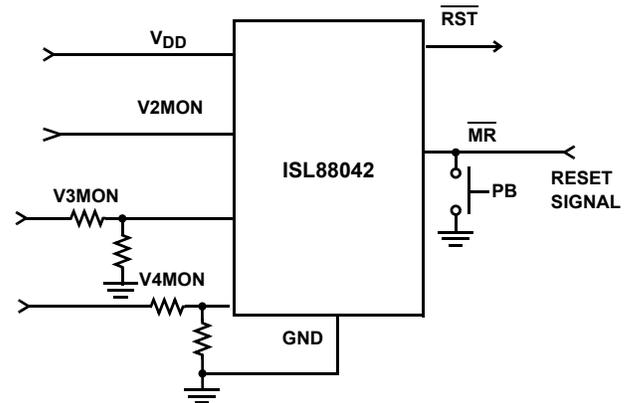


FIGURE 1. TYPICAL APPLICATION DIAGRAM

**Principles of Operation**

The ISL88042 device provides those functions needed for monitoring critical voltages, such as power-supply and battery functions in microprocessor systems. It provides such features as Power-On Reset control, supply voltage supervision, and Manual Reset Assertion. The integration of all these features along with competitive reset threshold accuracy and low power consumption, makes the ISL88042 device suitable for a wide variety of applications needing multi-voltage monitoring. See Figure 1 for the “Typical Application Diagram”.

**Low Voltage Monitoring**

During normal operation, the ISL88042 monitors the voltage levels of V<sub>DD</sub>, V2MON, V3MON and V4MON. If the voltage on any of these four inputs falls below their respective voltage trip points, a reset is asserted ( $\overline{\text{RST}}$  = low) to prevent the microprocessor from operating during a power failure or brownout condition. This reset signal remains low until the voltages exceeds the voltage threshold settings for the reset time delay period t<sub>POR</sub>.

The ISL88042 allows users to customize the minimum voltage sense level for two of the four monitored voltages. For example, the user can adjust the voltage input trip point (V<sub>TRIP</sub>) for the V3MON and V4MON inputs. To do this, connect an external resistor divider network to the VxMON pin in order to set the trip

point to some other voltage above 600mV according to Equation 1:

$$V_{TRIP} = 0.6V \times R_1 + R_2/R_2 \quad (EQ. 1)$$

**Power-On Reset (POR)**

Applying power to the ISL88042 activates a POR circuit, which makes the reset pin(s) active (i.e. RST goes high while  $\overline{RST}$  goes low). These signals provide several benefits:

- They prevent the system microprocessor from starting to operate with insufficient voltage.
- They prevent the processor from operating prior to stabilization of the oscillator.
- They ensure that the monitored device is held out of operation until internal registers are properly loaded.
- They allow time for an FPGA to download its configuration prior to initialization of the circuit.

The reset signal remains active until  $V_{DD}$  rises above the minimum voltage sense level for time period  $t_{POR}$ . This ensures that the supply voltage has stabilized to sufficient operating levels.

**Manual Reset**

The manual-reset input ( $\overline{MR}$ ) allows the user to trigger a reset by using a push-button switch or by signaling the input low. The  $\overline{MR}$  input is an active low debounced input. Reset is asserted if the  $\overline{MR}$  pin is pulled low to less than 100mV for the minimum  $\overline{MR}$  pulse width or longer while the push-button is closed. After  $\overline{MR}$  is released, the reset output remains asserted low for  $t_{POR}$  (200ms) and then is released.

Figures 2 and 3 illustrate the ISL88042's operation.

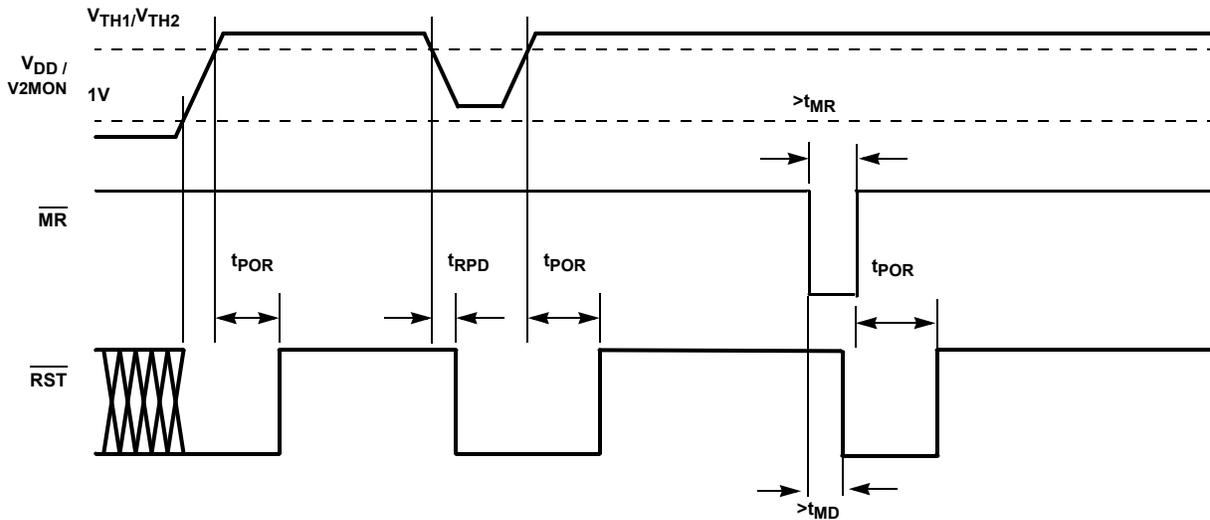


FIGURE 2. POWER SUPPLY MONITORING DIAGRAM

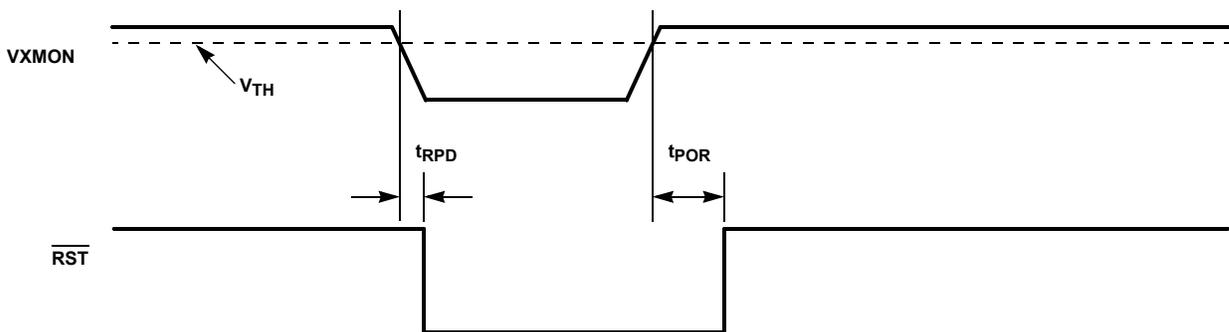


FIGURE 3. VOLTAGE MONITORING DIAGRAM

**The ISL88042EVAL1Z and Applications**

The ISL88042EVAL1Z supports all variants of the ISL88042 devices, enabling evaluation of basic functional operation and common application implementations. Figure 10 illustrates the ISL88042EVAL1Z in schematic and photographic forms. The ISL88042EVAL1Z is populated with the ISL88042IRTEEZ ( $V_{DD} V_{TH1}$  and  $V_{2MON} V_{TH2} = 2.90V$ ).

With adequate bias on the two preset and the two adjustable monitor inputs the  $\overline{RST}$  output will release to pull high indicating that all supplies are compliant for a minimum of  $t_{POR}$ . For the ISL88042EVAL1Z as shipped, the  $V_{DD}$  and  $V_{2MON}$  nominal thresholds are as previously noted with the voltage thresholds being monitored by  $V_{3MON}$  and  $V_{4MON}$  being left open for programming via the non populated resistor dividers.

**Typical Performance Curves**

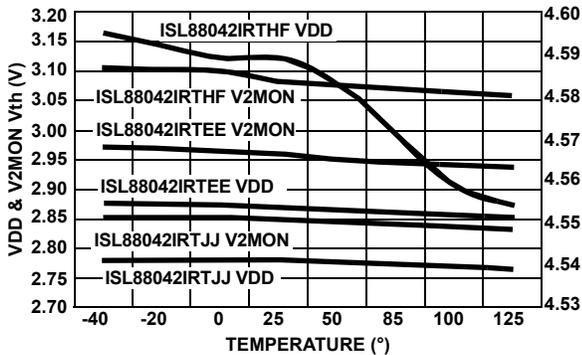


FIGURE 4. VDD and V2MON Vth vs TEMPERATURE

**Special Application Considerations**

Using good decoupling practices on bias and other monitoring inputs will prevent transients (i.e. due to switching noises and short duration droops in the supply voltage) from causing unwanted resets.

In unusually noisy environments or situations where unwanted signals may be injected into the adjustable  $V_{MON}$  inputs, lowering the node impedance and/or positioning a small valued filter capacitor as close to the pin as possible can increase noise immunity.

Although the internal ISL88042 threshold references are guaranteed over the full temp range, accuracy errors due to external component tolerances and distribution losses will occur. High tolerance resistors and layout for extreme accuracy and critical performance must be considered.

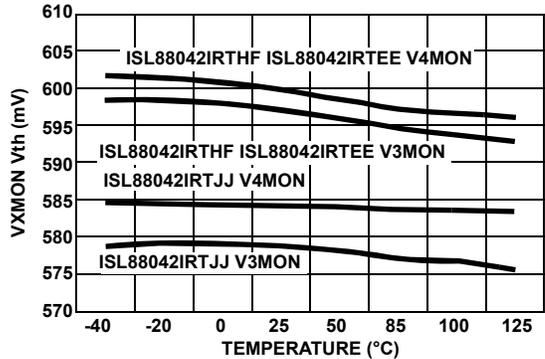


FIGURE 5. V3MON and V4MON Vth vs TEMPERATURE

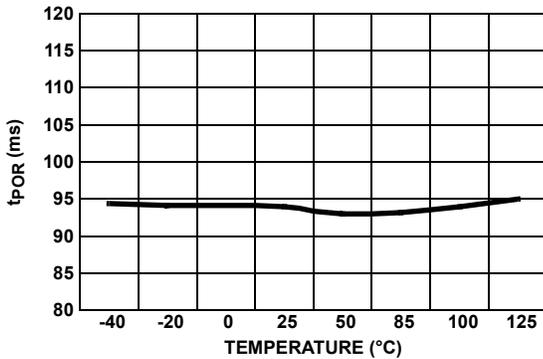


FIGURE 6.  $t_{POR}$  vs TEMPERATURE

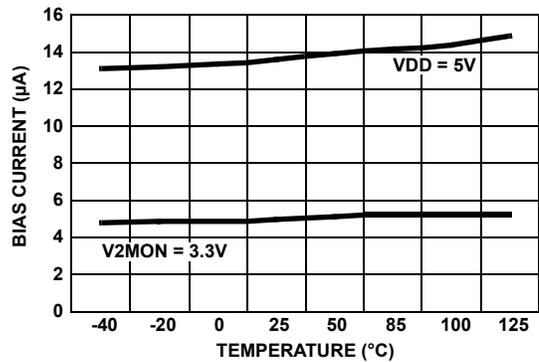


FIGURE 7. BIAS CURRENT vs TEMPERATURE

Typical Performance Curves

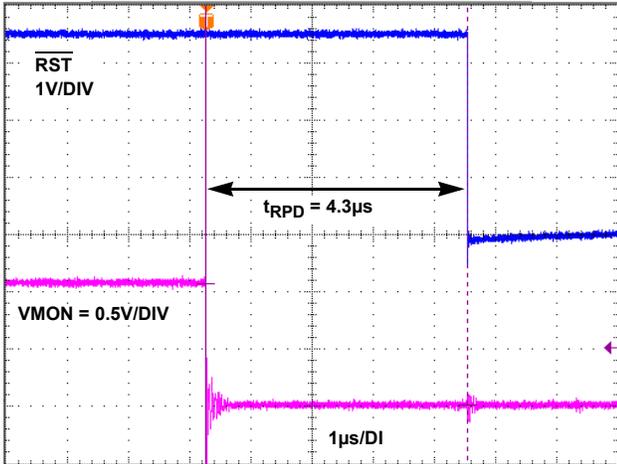


FIGURE 8. ISL88042  $t_{RPD}$

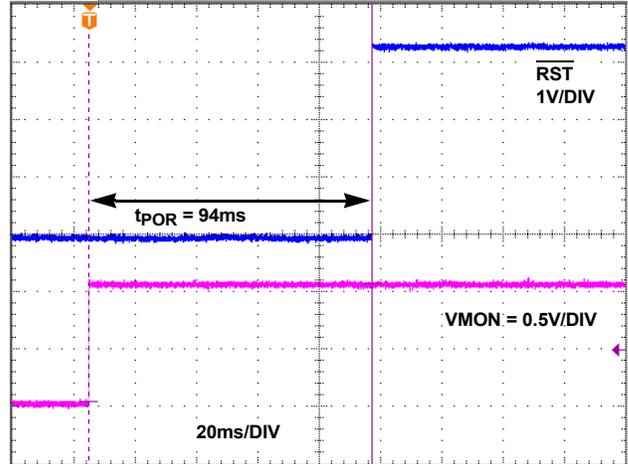


FIGURE 9. ISL88042  $t_{POR}$

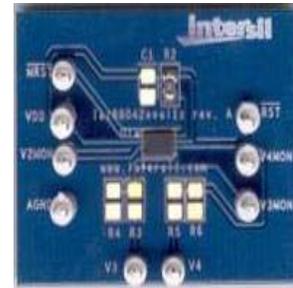
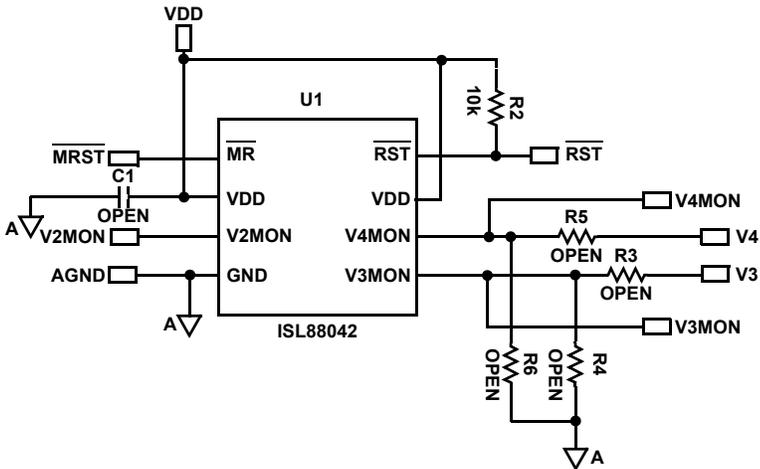


FIGURE 10. ISL88042EVAL1Z SCHEMATIC AND PHOTOGRAPH

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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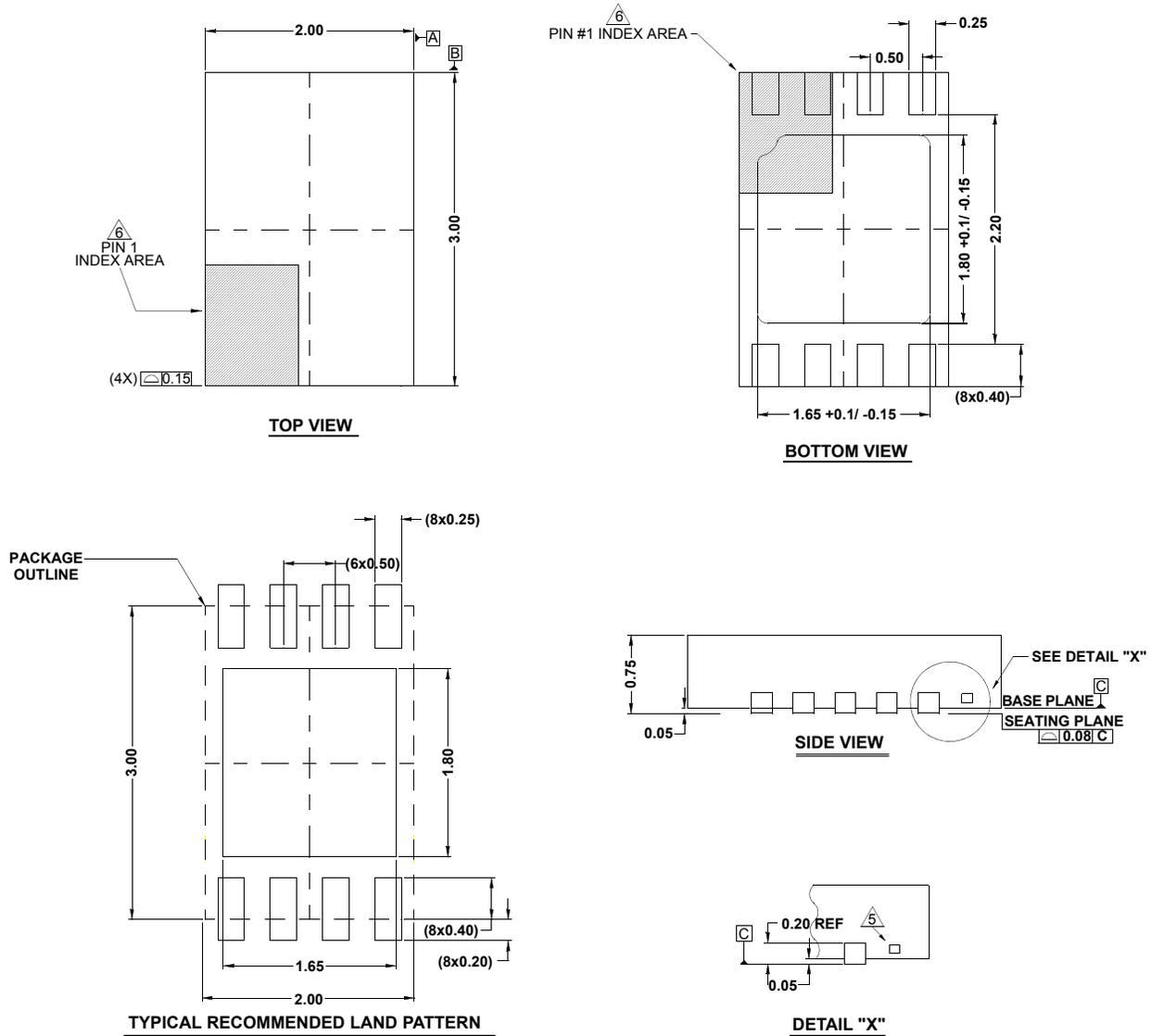
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## Package Outline Drawing

### L8.2x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE WITH E-PAD

Rev 1, 06/09



#### NOTES:

- Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
- Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
- Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
- Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.32mm from the terminal tip.
- Tiebar shown (if present) is a non-functional feature.
- The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.